TSVV-07 requests for ACH support

Code Name	Tasks required to ACH	ACH cat.	PMs/ year	Priority 2021	Priority 2022	Details/Comments
BIT-1D, BIT-3D	Code adaptation to IMAS, focusing firstly on IMAS compatible outputs	Cat II. (IM)	2.5	Low	Low to Medium	One might have set all IMAS tasks to low priority, however it is very difficult to say how much effort it will be for complex codes to make them IMAS compatible (input-output), so better to start earlier.
ERO2.0	Improved parallelization, such as e.g. compiler optimization and GPU	Cat I. (HPC)	1.5	High	High	Xavier Saez from BSC (ACH CIEMAT) is in charge of ERO2.0 support in the frame of expiring HLST, respective proposal is available, so probably no need to repeat details here. High priority since ongoing project, better to keep the grip.
ERO2.0	Code adaptation to IMAS, focusing firstly on IMAS compatible outputs	Cat II. (IM)	2.5	Low	Low to Medium	See comments for BIT.
MEMOS-U	Improvement of code architecture, modularity, memory usage	Cat I. (HPC)	1.5	Low	Medium to High	Employs the finite difference method solving coupled Navier-Stokes and heat convection-diffusion equations. The code is already parallelized and runs on IO clusters, but would benefit from further parallelization and optimization.
MEMOS-U	Code adaptation to IMAS, focusing firstly on IMAS compatible outputs	Cat II. (IM)	1.5	Low	Low to Medium	See comments for BIT.
MIGRAINe	Ensure HPC compatibility of the effective parallelization of serial simulations	Cat I. (HPC)	0.8	Medium	High	Being an ODE solver, MIGRAINe is inherently serial. Effective parallelization can be achieved by splitting the simulated trajectory batches. Code parallelization & optimization necessary to ensure compatibility with HPC clusters.
MIGRAINe	Code adaptation to IMAS, focusing firstly on IMAS compatible outputs	Cat II. (IM)	1.5	Low	Low to Medium	See comments for BIT.
RAVETIME	Upscaling from cluster-parallel to HPC-parallel and GPU-enabling	Cat I. (HPC)	1.2	Low	Low	RAVETIME is a parallel finite-volume 3D transport code designed to take advantage of developments within the European Exascale computing project VECMA on UQ methods. Deliverables from 2024.
RAVETIME	Code adaptation to IMAS, focusing firstly on IMAS compatible outputs	Cat II. (IM)	0.5	Low	Low	Probably from 2024.
Retention codes	A framework for effective parallelization at a later stage of the project	Cat I. (HPC)	1	Low	Low	Probably from 2024.
Retention codes	Code adaptation to IMAS, focusing firstly on IMAS compatible outputs	Cat II. (IM)	1	Low	Low	Probably from 2024.
SDTrimSP-1D, SDTrimSP-3D	Upscaling from cluster-parallel to HPC-parallel	Cat I. (HPC)	1.2	Low	Medium to High	Monte-Carlo codes for transport of ions in matter using binary collisions approximation.
SDTrimSP-1D, SDTrimSP-3D	Code adaptation to IMAS, focusing firstly on IMAS compatible outputs	Cat II. (IM)	1	Low	Low	Probably from 2024.
SPICE-2D, SPICE-3D	Upscaling from cluster-parallel to HPC-parallel	Cat I. (HPC)	1.2	High	High	Particle-in-Cell codes. Have already received support from HLST IPP (Serhiy Mochalskyy from Garching, Roman Hatzky). Parallel Poisson solver in 3D needs some bug fixes. Parallel Poisson in 2D is desired (is not straigt-forward).
SPICE-2D, SPICE-3D	Code adaptation to IMAS, focusing firstly on IMAS compatible outputs	Cat II. (IM)	1.5	Low	Low to Medium	See comments for BIT.
Interatomic potential development	Optimization and GPU-enabling	VTT	1.2	Low	Medium	VTT ACH because it is in-house for the respective group. Deliverables from 2023.

TSVV-07 Cat.2 IMAS PM/year	TSVV-07 Cat.2 IMAS ppy/year	TSVV-07 Cat.2 IMAS ppy total
12.0	1.00	5.00
+	+	+
TSVV-07 Cat.1 HPC PM/year	**TSVV-07 Cat.1 HPC ppy/year**	**TSVV-07 Cat.1 HPC ppy total**
9.6	0.80	4.00
=	=	=
TSVV-07 Total PM/year	**TSVV-07 Total ppy/year**	**TSVV-07 Total ppy total**
21.6	1.80	9.00