Pr16: Silicon optics steady state magnetic field sensor

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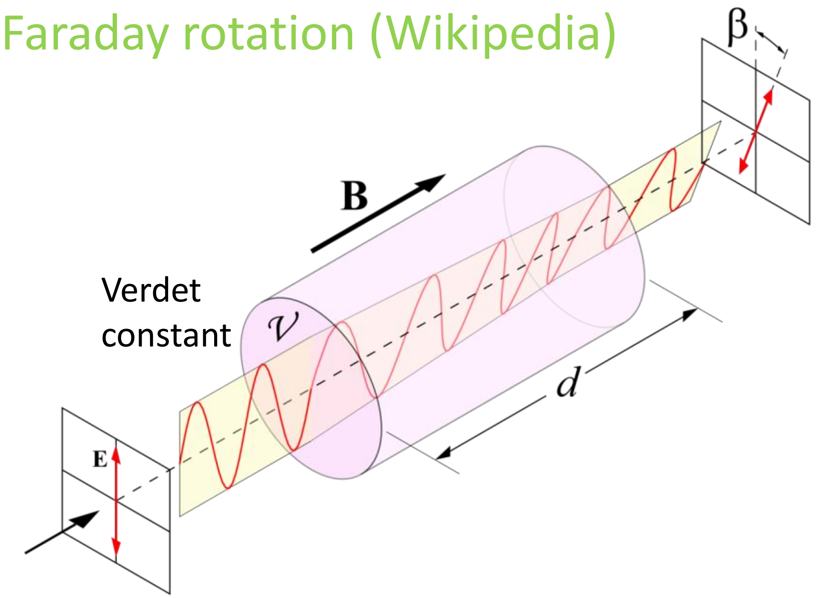
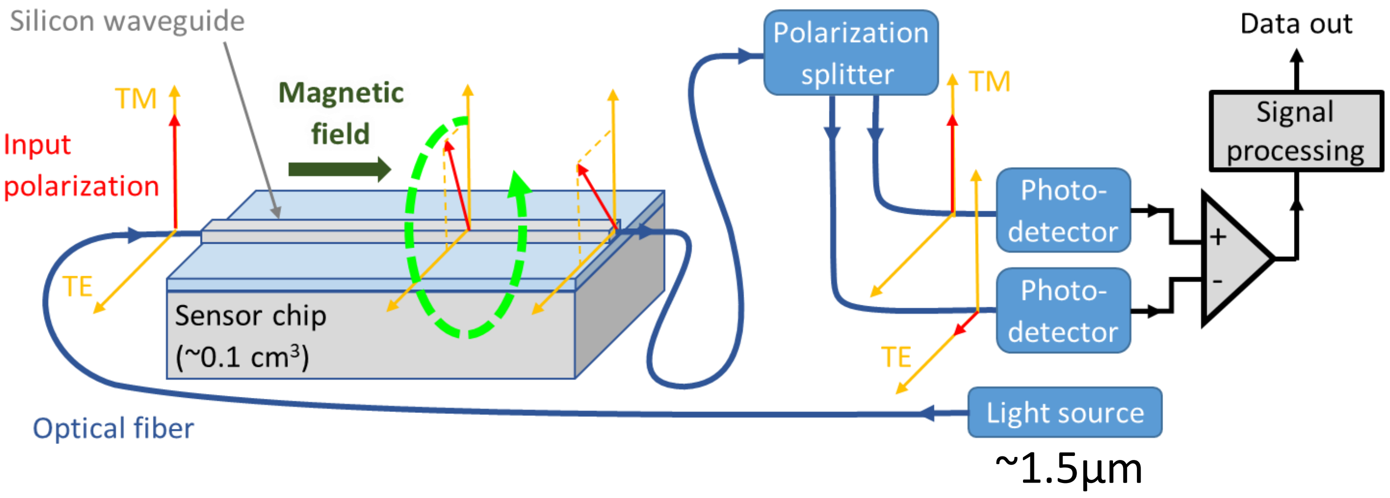
Measurement concept

Faraday rotation (Wikipedia)



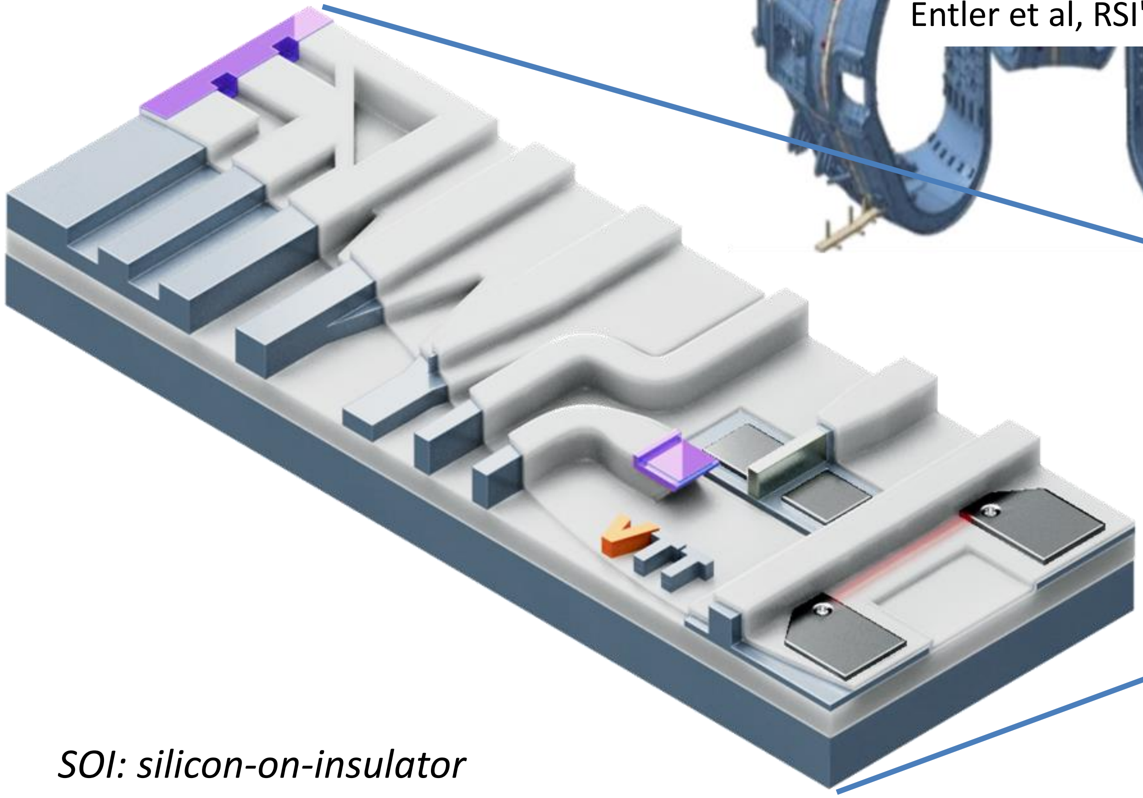
Sensor on silicon (simplified schematic)

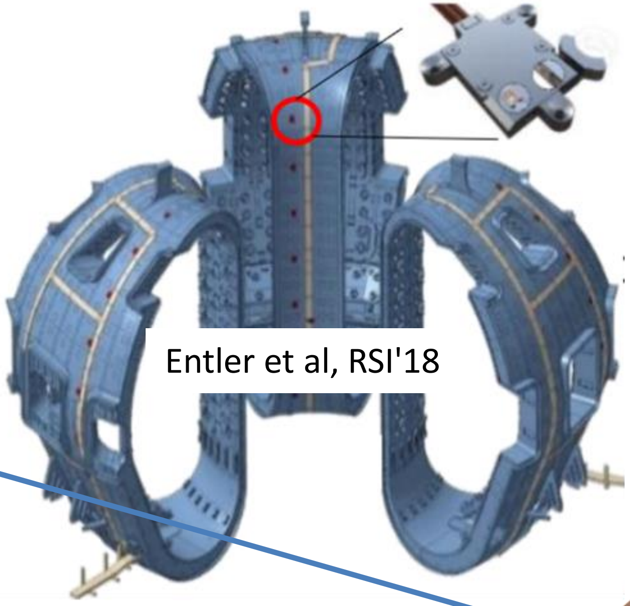


- **Aim**: develop a prototype steady state magnetic field sensor
- **Physics principle**: Faraday rotation of light under magnetic field influencing the output of an integrated polarization splitter
- **Technology**: Photonic integrated circuit (PIC) based on 3 µm thick silicon-on-insulator (SOI) waveguides
- **Speciality**: Folded waveguides and mirror-based U-bends to accumulate Faraday rotation, novel mirror-based polarization splitters, and a method to avoid the impact of unwanted Faraday rotation in input/output fibers

Big picture

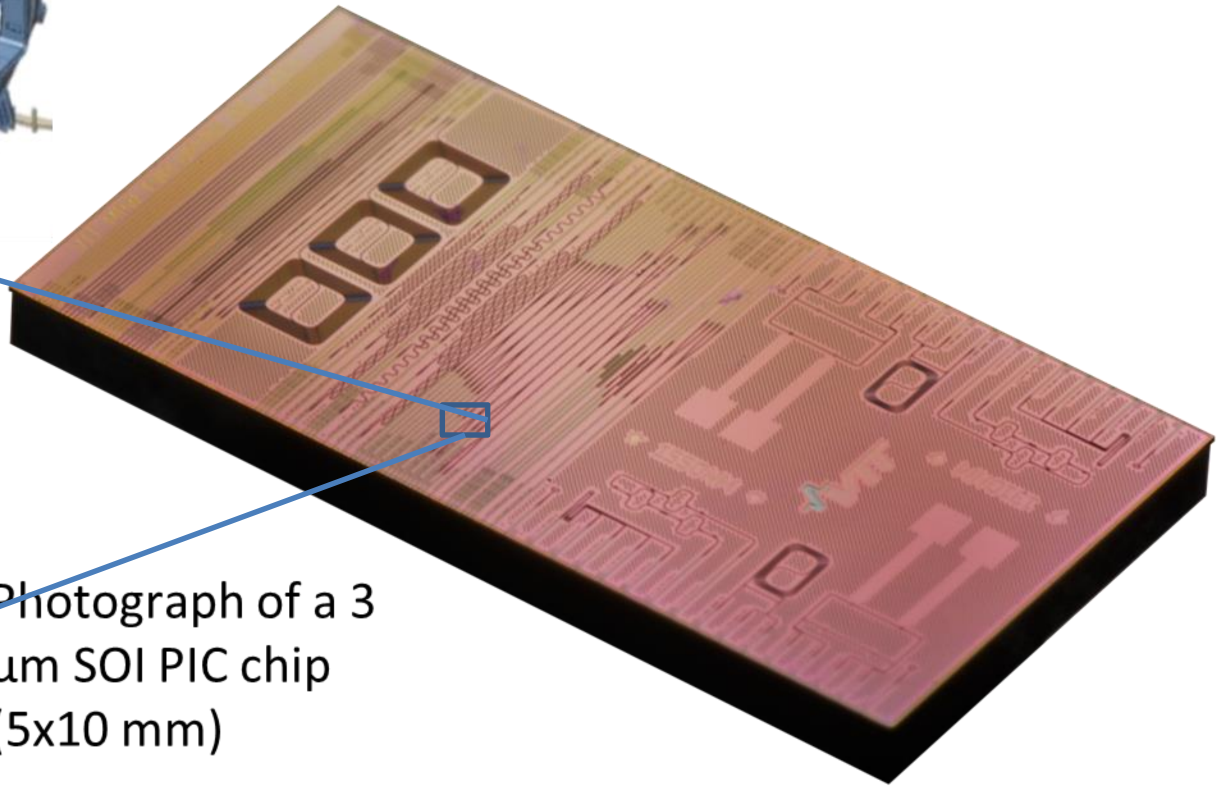
3 µm SOI PIC platform with passive and active functions (schematic)





Entler et al, RSI'18

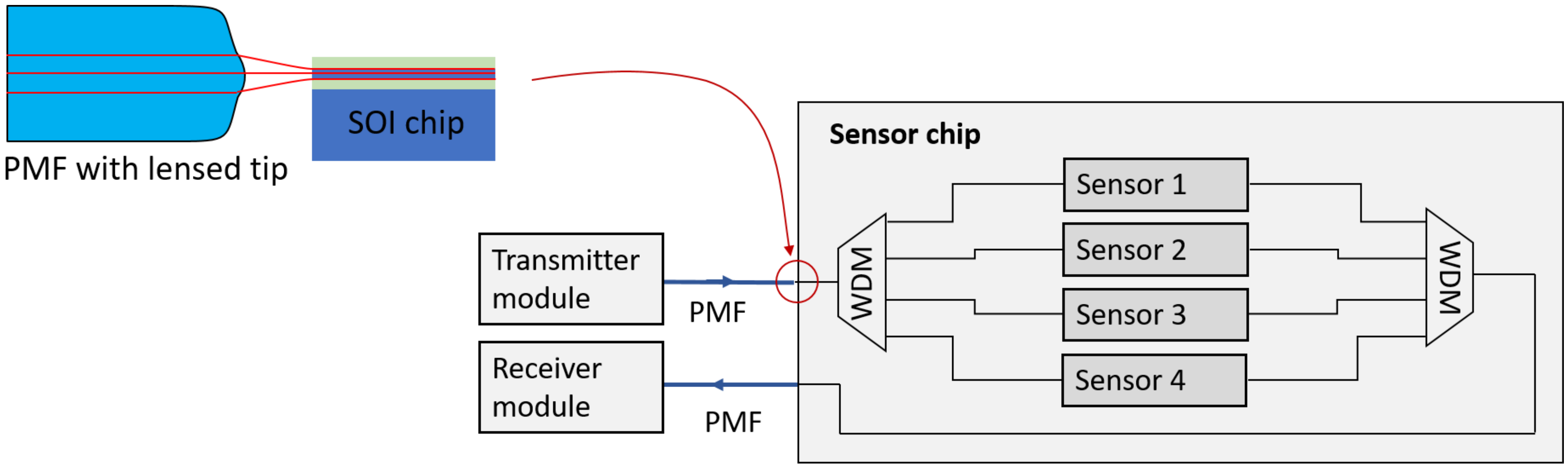
Illustration of a tokamak reactor with a (conventional) magnetic field sensor in one potential place for magnetic field measurement



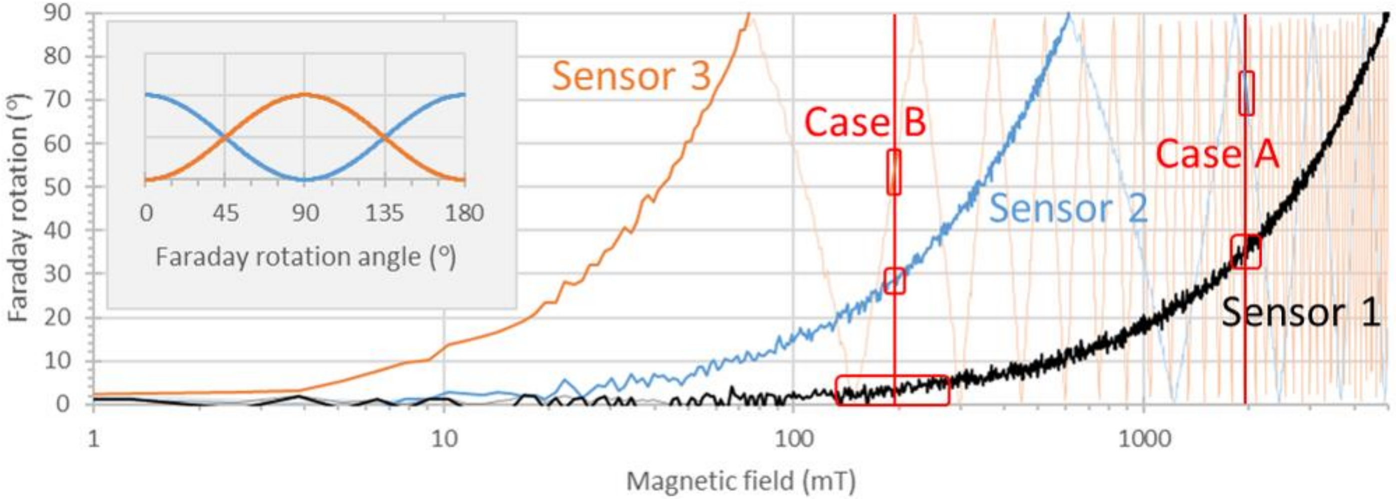
Photograph of a 3 µm SOI PIC chip (5x10 mm)

SOI: silicon-on-insulator
PIC: photonic integrated circuit

Multiple sensors for resolution



- Faraday rotation should be in the range of 1-89 degrees to for unambiguous magnetic field measurement
- Need to use 3-4 sensors on to obtain targeted performance (5T +/- 4mT)



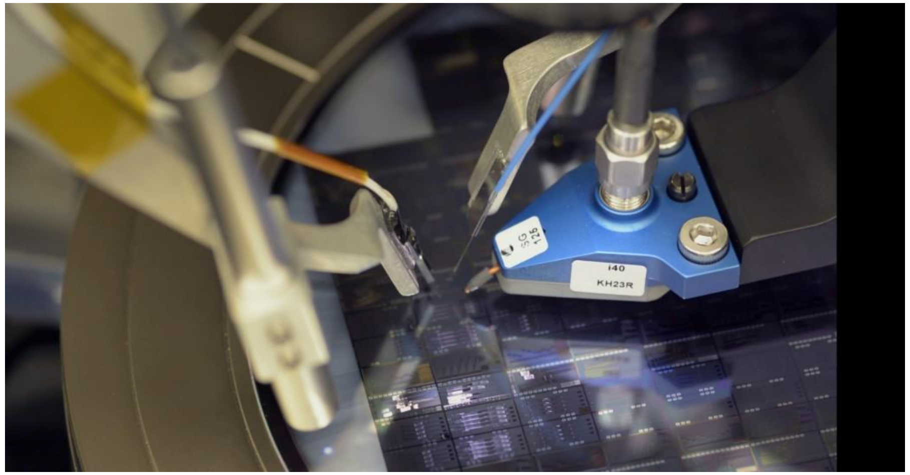
Micronova facility

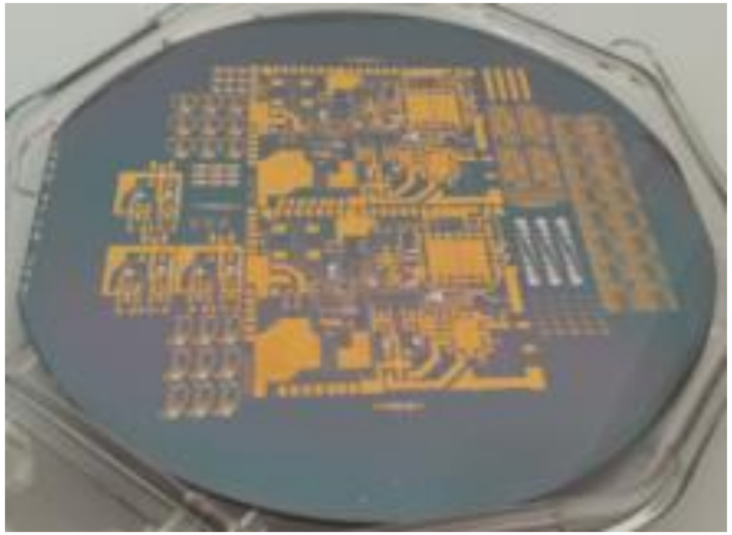
- Micronova is a research centre jointly run by the VTT Technical Research Centre of Finland and Aalto University
- Provides micro- and nanofabrication facilities for the development of microelectronic, **photonic**, microsystems and nanoelectronic components and devices.
- The biggest in the Nordic countries, Micronova's R&D cleanroom facilities in Otaniemi, Espoo, cover 2,600 m2.
- The facility consists of two large semiconductor manufacturing cleanrooms and other laboratories for processing, testing and characterization. The cleanrooms contain semiconductor processing equipment for lithography, etching and deposition as well as test and measuring equipment such as SEMs. In total there are some 200+ pieces of equipment that are used across a range of technology platforms.
- They are used by researchers from VTT, Aalto University and other universities as well as several companies.

Multi-project wafer (MPW) runs

- Multiple projects are combined on a single large wafer to share overhead costs
  - lower cost but longer wait
- Full MPW process flow takes 2-8 months, depending on process complexity
  - here 3-6 months is needed
- Typically 2 MPW rounds are made per year
  - minimum iteration cycle ~6 months
- masking, lithography, chemical vapour deposition, oxidation, …

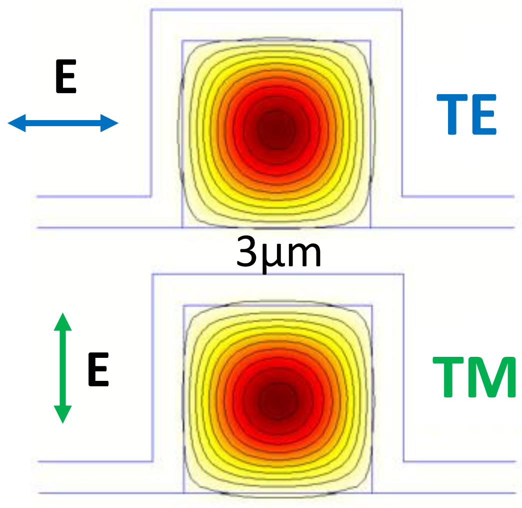
Wafer-level testing of different chip designs on an MPW wafer

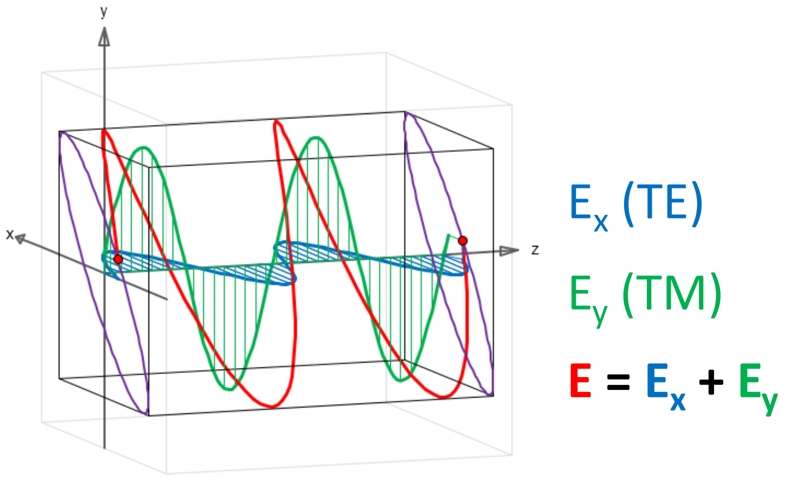




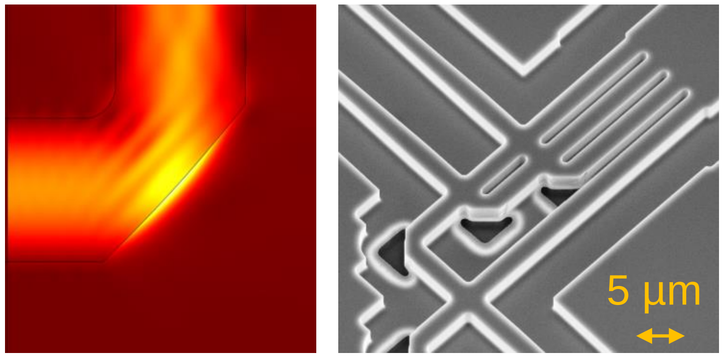
Design of silicon waveguide components

- Light primarily propagates in the fundamental mode of the SOI waveguide (with only one intensity maximum in the waveguide cross-section)
- Fundamental mode is further split into two polarization modes that normally (without Faraday rotation) propagate independently from each other: TE and TM modes have the electric field oriented horizontally and vertically, respectively
- Waveguide geometry and stress cause birefringence that represents the speed-difference of the TE and TM modes (causing mode interference)
- Waveguide modes and light propagation in waveguide circuits (PICs) is simulated with commercial simulation software (PhotonDesign, COMSOL etc.)





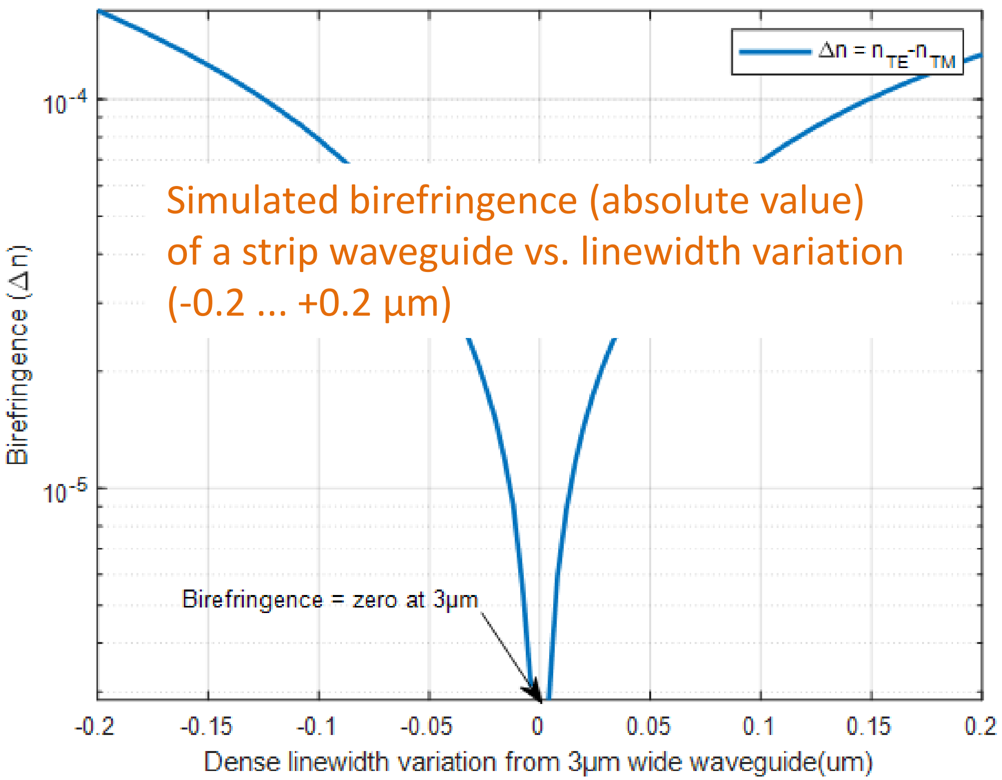
Cross-sections and propagation of TE and TM modes

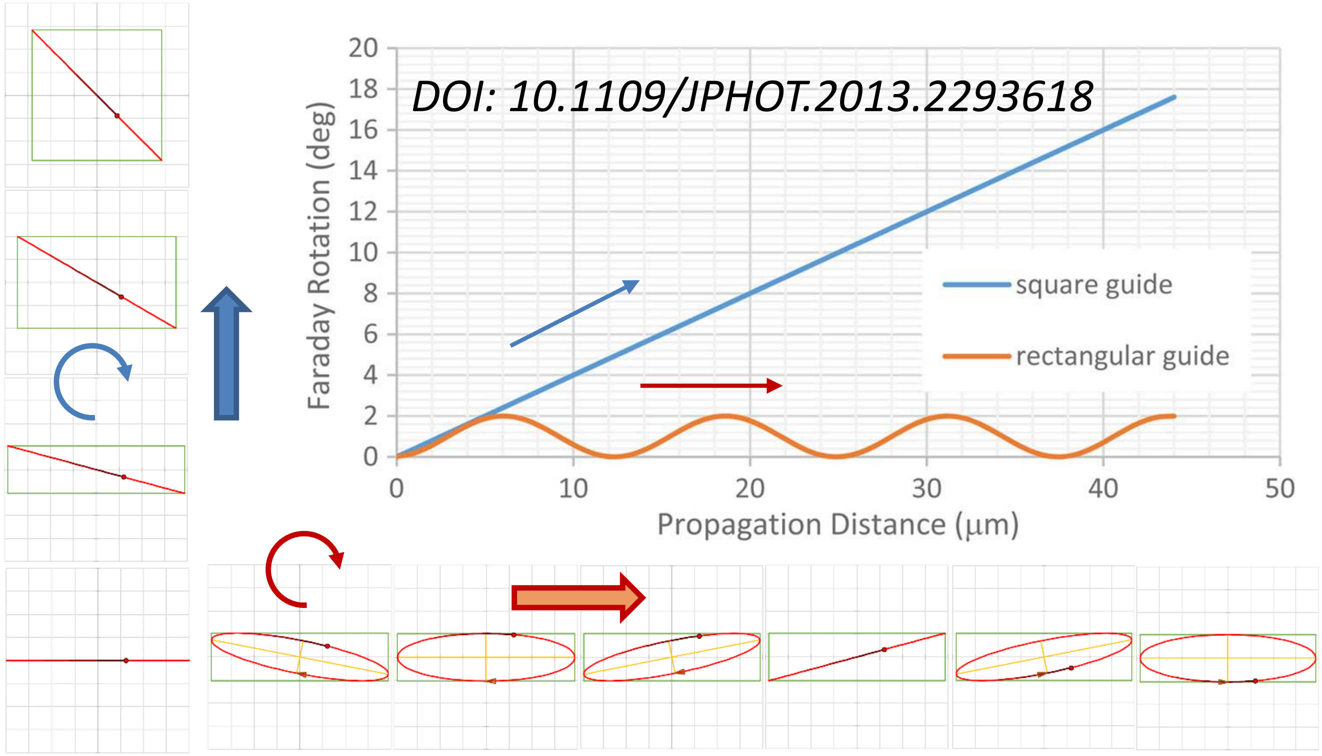


Simulated and fabricated waveguide mirrors

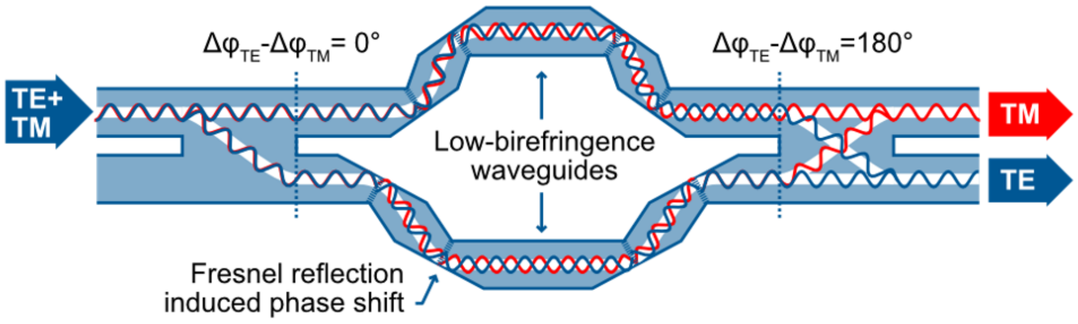
Task 1: make zero birefringence waveguides

- Zero birefringence of waveguides is needed for efficient Faraday rotation
- 3 µm wide strip waveguide can produce zero birefringence, but needs good linewidth control
- Methods for precise measurement of small birefringence have been developed

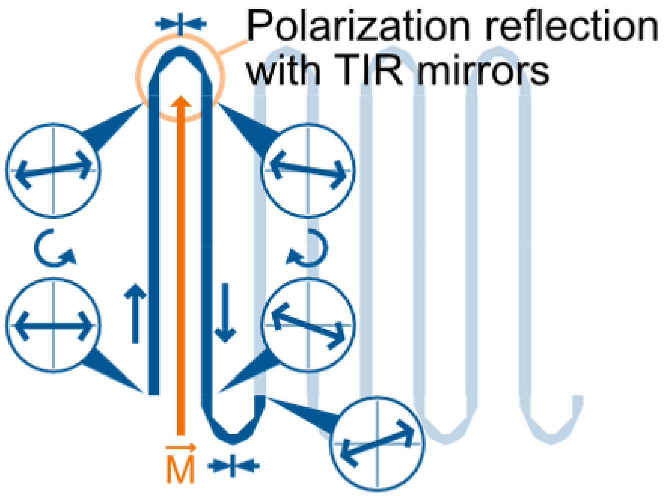




Building blocks for silicon waveguides

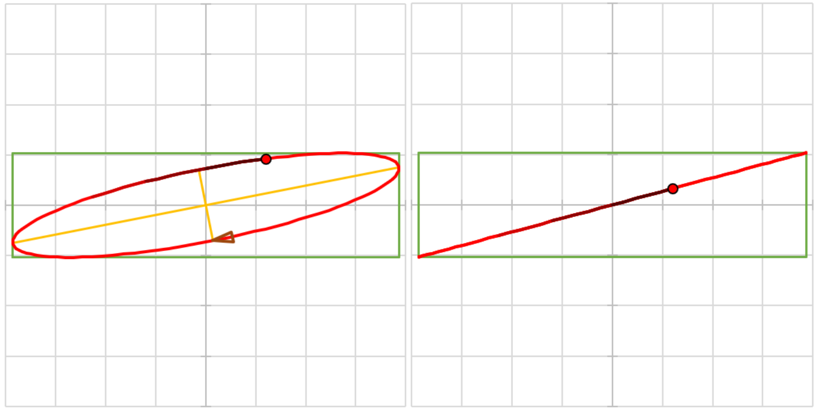


- Novel polarization beam splitter (PBS)
  - Separates TE and TM polarizations
  - Based on wavelength-independent and polarization-dependent phase shifts in total internal reflection (TIR) mirrors
  - First polarization splitters successfully demonstrated
  - New test structures designed and in fabrication
- Novel Faraday rotator
  - Long waveguide folded with small U-turns
  - Polarization rotation in straight sections
  - Polarization is reflected in the U-turns due to TIR-mirrors, allowing to accumulate polarization rotation
  - Test structures designed and fabrication in process
- Novel concept to multiplex signals on the same chip
  - Confidential, to be disclosed later

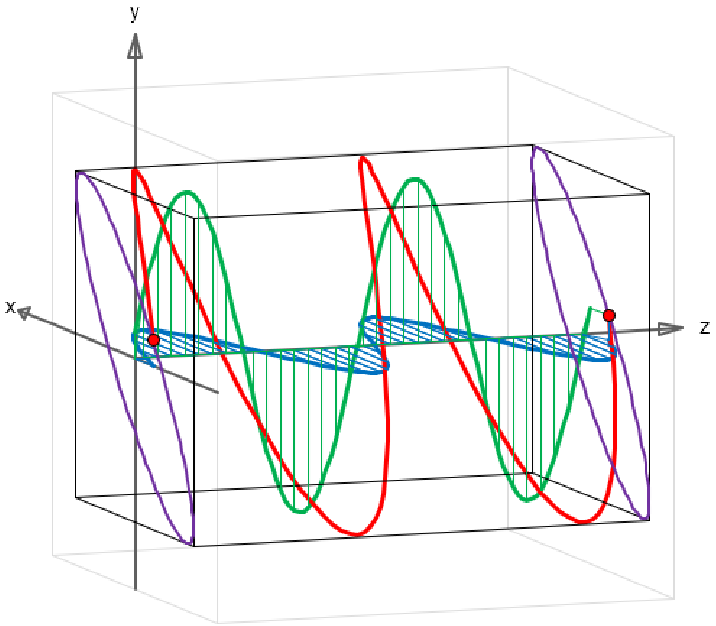


Development of design and simulation tools

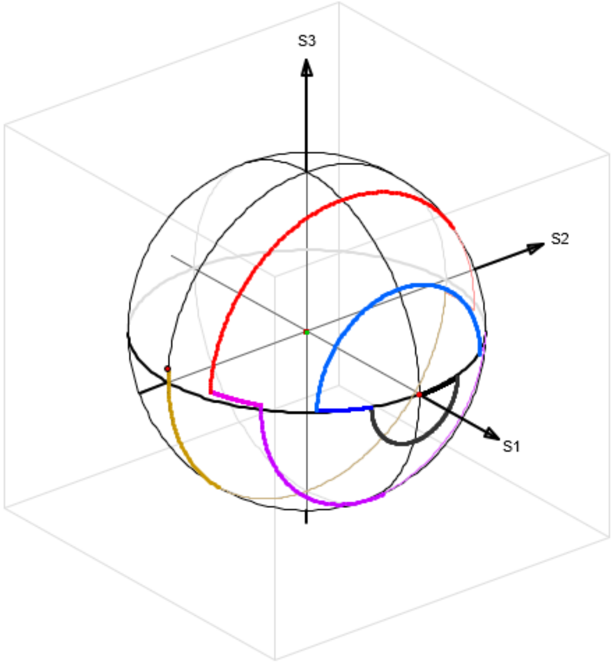
- Software tools have been developed for the design and simulation of polarization management components (Excel, Matlab, Python)
  - Polarization evolution in waveguides with zero and finite birefringence
  - Cascades of straight sections and U-turns
  - Compensation of imperfect polarization flipping in U-turns



Polarization ellipses



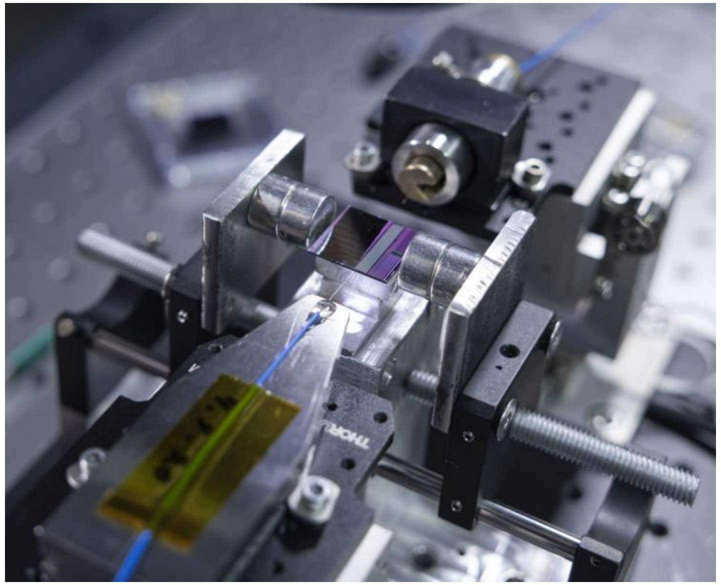
Field propagation simulation



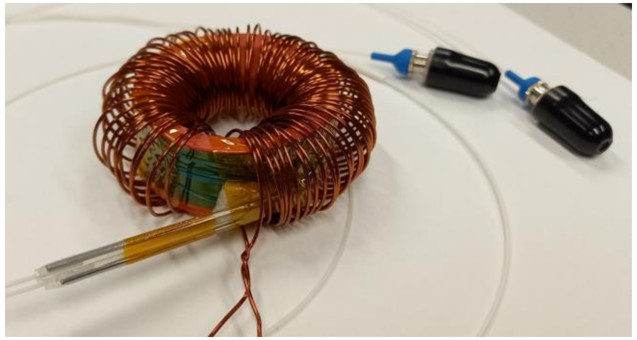
Poincaré simulation

Measurement setup for magnetic field measurements

- Permanent magnets have been used for silicon waveguide measurements
  - Up to 6 cm silicon waveguides (birefringence not yet fully minimized)
  - 0.2 T magnetic field (magnet upgrades planned)
- Faraday effect has been demonstrated with optical fiber and electromagnet
  - 100 m long fiber
  - 4 mT magnetic field



Prototype sensor circuits will be characterised using on campus PPMS device capable of
B = 0 to 8T and T = –270 to +127 C automated scans



Optical fiber measurements

Summary

- Initial research focus is on
  - Zero birefringence development
    - Enables efficient Faraday rotation
  - Polarization-flipping U-turns
    - Enables Faraday rotation accumulation in opposite directions
  - Polarization splitters
    - Provides stable input polarization before Faraday rotation
    - Provides readout for the amount of Faraday rotation
  - Design and simulation of the PIC (photonic integrated circuit) components
    - New simulation tools developed
    - Test chips designed
- Silicon waveguide building blocks are in the process and first wafer will be ready in late 2021 or early 2022
  - Each building block will be tested separately
- In 2022, more advanced PICs and the combination of Faraday rotation and polarization splitters will be demonstrated