TSVV - ACH meeting

The big picture

- Goal: To produce scientific codes that can use Tier-0 systems efficiently.
- GPUs are dominant at the top.
- What do we need to get there?

HPC first principles - Roofline model and memory wall

HPC means reducing Time To Solution (more science, increased accuracy, less energy used…)

Roofline model: (if latencies are covered) **TTS is proportional to the inverse of memory** or **arithmetic throughput** (**GB/s or Gflops/s**), which is determined by the arithmetic intensity of your algorithm (and the memory wall).

Little's law: throughput = **parallelism**/latency or 1 /throughput = latency/**parallelism** \sim TTS

Reducing TTS means exposing parallelism in scientific software

Research Codes vs. HPC codes: Scope

How do we make sure to reach maximum performance?

fluid drift-reduced Braginski equations,
$$
k_{\perp}^{2} \gg k_{\parallel}^{2}
$$
, $d/dt \ll \omega_{ci}$
\n
$$
\frac{\partial \eta}{\partial t} = -\frac{1}{2} [\phi, \eta] + \frac{2}{e\theta} [G(\rho_{b}) - e\eta G(\phi)] - \nabla_{1} (\eta v_{\parallel \phi}) + D_{\alpha} (\eta) + S_{\alpha} + \eta_{\alpha} v_{\alpha} - n v_{\alpha \alpha}
$$
\n(1)
\n
$$
\frac{\partial \zeta}{\partial t} = -\frac{1}{2} [\phi, \omega] - v_{\parallel} \nabla_{\parallel} \bar{\omega} + \frac{\theta^{2}}{m_{\parallel} \theta} \nabla_{\parallel} \bar{\mu} + \frac{2B}{m_{\parallel} \theta} G(\rho) + D_{\alpha} (\zeta) - \frac{R_{\theta}}{m_{\parallel} \omega} \omega_{\omega} \omega_{\omega}
$$
\n(2)
\n
$$
\frac{\partial v_{\parallel}}{\partial t} = -\frac{1}{2} [\phi, v_{\parallel}] - v_{\parallel} \nabla_{\parallel} v_{\parallel} + \frac{\theta}{m_{\parallel} \theta} \nabla_{\parallel} \phi - \frac{T_{b}}{m_{\parallel} \theta} \nabla_{\parallel} \phi - \frac{T_{b}}{m_{\parallel} \theta} \nabla_{\parallel} \eta_{\alpha} + T_{\theta} v_{\alpha} (v_{\parallel \theta})
$$
\n(3)
\n
$$
\frac{\partial v_{\parallel}}{\partial t} = -\frac{1}{2} [\phi, v_{\parallel}] - v_{\parallel} \nabla_{\parallel} v_{\parallel} - \frac{1}{m_{\parallel} \theta} \nabla_{\parallel} \rho + D_{v_{\parallel}} (v_{\parallel}) + \frac{T_{\theta}}{m_{\parallel} \theta} (v_{\alpha} + v_{\alpha}) (v_{\parallel \vert} - v_{\parallel \vert})
$$
\n(4)
\n
$$
\frac{\partial r_{\parallel}}{\partial t} = -\frac{1}{2} [\phi, T_{b}] - v_{\parallel} \nabla_{\parallel} T_{b} + \frac{4T_{b}}{3\theta} \left[\frac{T_{a}}{n} C(\eta) + \frac{7}{2} C(T_{b}) - eC(\phi) \right] + \frac{2T_{b}}{3\theta} \left[\frac{0.71}{\theta} \nab
$$

How to transition towards HPC codes

Performance analysis in-depth.

- Benchmarks definition and strategy.
- Profiling.
- Identification of bottlenecks.
- Translation into computational patterns.

Codes and bottlenecks - benchmarks strategy

- Goal: To understand the application's behavior as a function of the resources.
- Many HPC call for resources requires representative benchmarks showing performance/scalability of the application.
- Usually this activity is performed "by hand".
- From last meeting: "It would be interesting to introduce more automation in the benchmarking activity".

Towards automatic benchmarks: Idea

Towards automatic benchmarks - generation

The configurations represent the resources (threads, MPI)

The configuration are application and machine dependent.

Towards automatic benchmarks - analysis of the application log

- If the application has timers it is possible to extract them.
- Then, we can sort the timers in ascending order.
- And, by changing the resources.

Towards automatic benchmarks - analysis of the profiler log

● We can also use profilers to get more information on the application bottlenecks.

Knowing the tool: VTUNE

1 THREAD

● Tools like VTUNE provide a lot of information.

\odot Top Hotspots

This section lists the most active functions in your application. Optimizing these hotspot functions typically results in improving overall application performance.

*N/A is applied to non-summable metrics.

Analysis Configuration Collection Log Summary Bottom-up Caller/Callee Top-down Tree Platform

\odot Elapsed Time \odot : 184.023s

\odot Top Hotspots

This section lists the most active functions in your application. Optimizing these hotspot functions typically results in improving overall application performance.

*N/A is applied to non-summable metrics.

OVERVIEW OF THE CODES

- GRILLIX
- GBS
- SOLEDGE3X

GRILLIX

- Current status:
	- Compilation:
		- Dependencies: cmake, mpi, openmp, hdf5, lapack, blas, netcdf
		- Tested on Izar@EPFL and Marconi: Worked out of the box.
	- Parallelization:
		- The poloidal planes are distributed with MPI
		- Each poloidal plane is parallelized with OpenMP
- Benchmark strategy:
	- The number of poloidal planes is fixed and distributed with MPI
	- For each poloidal plane is possible to increase the number of threads
	- Goal: To study the scalability of GRILLIX by increasing the number of threads, up to 1 MPI per NUMA socket.

GBS

- Current status:
	- Compilation:
		- Dependencies: cmake, mpi, openmp, hdf5, lapack, blas, petsc, hypre, AMGX
		- Successfully tested on a variety of architectures, including GPUs.
	- Solver:
		- Direct(MUMPS)
		- Iterative(PETSc, AMGX)
		- Parallelization:
			- MPI in the poloidal plane

- RHS computation:
	- Stencil operations memory bounded
	- Parallelization: MPI across the domain
- Benchmark strategy:
	- We usually increase the number of MPI task on the toroidal direction and fix the number of MPI tasks in the poloidal plane

TCV on SuperMUC-NG

SuperMUC-NG hardware

- 6480 Intel Skylake Xeon Platinum 8174
- 96GB DDR4 memory
- Network: Intel Omni-Path
- Setup: TCV at 0.9T, 100 timestep
	- **Turbulent mode**
	- $Nx = 300$, $ny = 600$, $nz = 128$
	- Solver: deflated GMRES
	- Preconditioner: Hypre/BoomerAMG

Time and speedup for 100 plasma iterations

x-y-z processor partition

2 node: 6x8x2 cores 32 nodes: 6x8x32 cores 4 nodes: 6x8x4 cores 64 nodes: 6x8x64 cores 8 nodes: 6x9x8 cores 128 nodes: 6x16x64 cores 16 nodes: 6x8x16 cores 256 nodes: 12x16x64 cores

AT **64 NODES** IT TAKES **0.45s/STEP TO SOLVE FULL TCV** → **~6M CORE HOURS** FOR THE FULL SIMULATION

JT60-SA on SuperMUC-NG

SuperMUC-NG hardware

- 6480 Intel Skylake Xeon Platinum 8174
- 96GB DDR4 memory
- Network: Intel Omni-Path

Setup: JT60-SA, 100 timestep

- Turbulent mode
- Nx = **1200**, ny = **2000**, nz = 300
- Solver: deflated GMRES
- Preconditioner: Hypre/BoomerAMG

9 (s/step)*10M(steps)*75(nodes)*48(cores/node) ~ 90M core/hours

● Current status:

- **○** Soledge3X relies on a mix explicit-implicit scheme
- It uses MPI+OpenMP
- it uses Petsc, Pastix, Hypre for implicit solvers

● Goals:

- profiling Soledge3X on SCITAS and Marconi clusters
- implement performance metrics to understand main bottlenecks
- use miniapp to investigate main bottlenecks and analyse performance in depth
- optimize and porting to GPU some parts of the code

Time-stepping scheme in Soledge3X

● Main loop algorithm regarding main CPU time-consuming routines

Parallelization in Soledge3X

- Spatial discretization:
	- \circ structured grid in the (ψ,θ,φ) coordinate system aligned with magnetic flux surfaces (ψ associated with the magnetic flux)
	- the solvers *evolveImplicitMomentum* and *evolveImplicitEnergy* are built using 2D stencils located in magnetic flux surface:
		- \rightarrow independent linear 2D mesh-based solvers are called for each value of ψ (magnetic flux surface)
	- however, the solver *evolveImplicitElectricPotential* is 3D mesh-based
- PETSC, PASTIX and HYPRE can be used for implicit solvers
- The domain is decomposed in zones for X-point geometries (see figure)
- MPI domain decomposition according to the (ψ,θ,φ) structured grid: the domain is in priority decomposed along the ψ direction (according to the magnetic flux surface workload), then along the θ direction
- MPI communicator for each magnetic flux surface (each value of ψ), useful for 2D mesh-based solvers
- OpenMP is used for each MPI process, except in PETSC and HYPRE solvers

Profiling setup

- Setup: Helvetios@SCITAS cluster
	- 2 Skylake processors running at 2.3 GHz, with 18 cores each
	- 192 GB of DDR3 RAM
	- Intel compiler
- Test case : circle 3D

 0.04

 0.02

 0.00

 -0.02

 -0.04

 0.36

Zone: 2
 ψ : 17

 0.38

 θ : 2

 $\mathbb{Z}\left[\mathfrak{m}\right]$

- \circ Npsi = 50, Ntheta = 500, Nphi = 50
- Petsc for all implicit solvers

 $R[m]$

- BiCGStab (Stabilized BiConjugate Gradient)
- AMG preconditioner
- Presence of wall

 T, e^- [eV] linear scale.

Profiling Soledge3X

● Main loop distribution for pure MPI parallelism

Strong scaling: more efficient when the number of MPI processes divides the number of magnetic flux surfaces

Strong scaling - pure MPI

#cores

Strong scaling

Weak scaling

Profiling with Scorep

- Main loop: Scorep analysis for 144 MPI processes
	- Communication efficiency (*maximum across all processes of the ratio between useful computation time and total run-time*):

CommE = maximum across processes (ComputationTime / TotalRuntime) = 0.94

● Load balance efficiency (*ratio between average useful computation time* - *across all processes and maximum useful computation time - also across all processes -* :

LB=avg(ComputationTime) / max(ComputationTime) = 0.71

Profiling with Scorep

● evolveImplicitPHI routine: MPI barrier take most of the time

Miniapps for linear solvers

- use of Miniapp (see Nicola's talk on solvers):
	- New routine in Soledge3X for dumping matrices in PETSC format for all implicit solvers
	- The Miniapp loads matrices and solves linear system with PETSC and AMGX (see Nicola's talk on solvers)
	- AMGX First tests:
		- the miniapp allows the comparison between Petsc and Amgx
		- AMGX converges for matrices corresponding to 2D implicit solvers ; for matrix corresponding to the 3D Electric potential implicit solver AMGX converges only for coarse mesh

--> need to investigate further AMGX parameters

● HYPRE - First tests: HYPRE with OpenMP installed on Scitas cluster. Use of miniapp to test the pinning of threads to cores. Need of OpenMP nested regions to couple OpenMP threads in Soledge3X and HYPRE threads.

First conclusions on Soledge3X profiling

- Conclusions
	- Profiling shows most of the computation time is spent within the implicit solvers
	- MPI parallel efficiency depends on the ratio of the number of MPI processes and the number of magnetic flux surfaces
	- OpenMP is quite efficient except for linear solvers (PETSC doesn't use threads !)
- Perspectives
	- Miniapp can help to test different linear solvers
	- Look at linear solvers using threads (Hypre ?)
	- Look at the MPI decomposition (depending in particular on the heterogeneous workload between magnetic flux surfaces and the presence of penalization mask to take into account walls)
	- Port to GPU some parts of the code
	- Overlap CPU/GPU computation
	- Intra-node optimization (OpenMP, vectorization)

intra-node profiling

● Intel-Vtune

Miniapps

- Definition: Standalone applications aimed to study specific problems.
- Usually we take the subroutines from the main codes and we turn them into standalone application.
- We need to:
	- Save the necessary data from the main codes, e.g. HDF5, NETCDF.
	- Isolate the subroutine and its dependencies (modules, libraries).
	- Create the Makefile or CMAKE.
- Advantages:
	- Easier to develop than the main codes.
	- Ideal for testing.
	- It's doable to perform tracing.
	- Facilitate the interaction with vendors.
- Disadvantages:
	- The modification have to be injected back to the main applications.
	- The miniapp and the main application have to be maintained separately.

Miniapps relevant to the community

- Elliptic solver.
- Stencil computation.

Elliptic Solver

- The solver/preconditioner used for the Poisson equation is one of the most critical bottleneck.
- Most of the solvers involved in this project are performed in the poloidal 2D plane, with the exception of the electric potential in Soledge3X.
- What are the main solver's components?
	- Matrix building.
	- RHS building.
	- Matrix solve.
- What miniapps:
	- Solver test: just perform Ax=b. A,b inputs.
		- Purpose: To compare different methods to solve the linear system.
	- Solver + matrix build: build the matrix and solver the system.
		- Purpose: To mimic what is done in the main codes.

Solver test

- For this miniapp we read from file the matrix and rhs.
- PETSc support for now

The MatSetFromOptions, VecSetFromOptions, KSPSetFromOptions allow a great degree of flexibility

The user specify a petscrc file

PETSCRC

-poisson ksp tvpe damres -poisson_pc_type hypre poisson_pc_hypre_type boomeramg -poisson ksp rtol 1e-7 -poisson ksp atol 1e-15 -poisson ksp reuse preconditioner ves poisson ksp initial quess nonzero ves· poisson pc hypre boomeramg strong threshold 0.25 poisson pc hypre boomeramg max levels 30 poisson pc hypre boomeramg coarsen type Falgout- $\frac{1}{2}$ poisson $\frac{1}{2}$ pc hypre boomeramg agg nl $\frac{1}{2}$ -poisson pc hypre boomeramg agg num paths 2 poisson_pc_hypre_boomeramg_truncfactor 0.2 poisson pc hypre boomeramg interp type ext+i

Solver test miniapp - Grillix testcase

- Data in CSR.
- Input: matrix and rhs.
- Information extraction fron netcdf.
- Integration with PETSc in Python.
- Fast prototyping.

Solver test - parameter scan

- 1) Explore the configurations by generate the possible permutations solver/preconditioner specified in the hyperparameters.json
- 2) Loop over the configurations, generate the slurm script and submit to the queue.

Solvers/Preconditioner scan

We did a scan of the possible permutations of solver/preconditioner in order to find the best performance for 1 poloidal plane

- Hypre preconditioner gives the best TTS across many solvers
- 1655 configuration tested
- Algebraic multigrid works well for these kind of solvers
- The permutations of the hypre/BoomerAMGX preconditioner parameters would require ~2M jobs
- We froze one parameter at a time for the most significant parameters in order to find the optimal configuration

TTS vs solver/preconditioner

- Setup: Reduced TCV at 0.9T
	- **Turbulent mode**
	- $Nx = 300$, $ny = 600$
	- 1 node of TAVE, KNL
	- 64 cores AVX512

Solver test - discussion

- The PETSc implementation works well but matrix and vectors have to be in the PETSc format.
- It is possible to build the matrix from other formats, e.g. CSR.
- Which format shall we use?

Matrix building and solver miniapp

- Goal: to optimize the time-to-solution of matrix building plus solver.
- Building the matrix can be an expensive operation. However, it can be optimized in many cases.
- Usually the matrix is built from stencil operations, typically memory bounded.
- Test case: GBS

The solver in GBS

- The matrix building:
	- \circ In GBS the poloidal plane has rectangular geometry and size (Nx, Ny).
	- For each point a 9 point stencil is computed, which then populate the matrix used by the solver.
	- Depending upon the solver used the matrix is built in different ways.
- The solver:
	- Direct MUMPS
	- Iterative CPU PETSC
	- o Iterative GPU AMGX

Matrix Assembly - PETSc CPU

DMDACreate2d

Creates an object that will manage the communication of two-dimensional regular array data that is distributed across some processors.

Synopsis

#include "petscdmda.h" <u>PetscErrorCode = DMDACreate2d(MPI Comm</u> comm,<u>DMBoundaryType</u> bx,<u>DMBoundaryType</u> b**y**,DMDAStencilT<u>ype</u> stencil type, PetscInt M, PetscInt N, PetscInt m, PetscInt n, PetscInt dof, PetscInt s, const PetscInt lx[], const PetscInt ly[], DM *da)

Collective

Input Parameters

- MPI communicator comm
- bx,by - type of ghost nodes the array have. Use one of DM BOUNDARY NONE, DM BOUNDARY GHOSTED, DM BOUNDARY PERIODIC. stencil_type- stencil type. Use either DMDA_STENCIL_BOX or DMDA_STENCIL_STAR
- global dimension in each direction of the array $M.N$
- corresponding number of processors in each dimension (or PETSC DECIDE to have calculated) $m.n$
- dof - number of degrees of freedom per node
- stencil width ϵ
- arrays containing the number of nodes in each cell along the x and y coordinates, or NULL. If non-null, these must be of length as m and n, and the corresponding m and n lx, ly cannot be PETSC DECIDE. The sum of the 1x[] entries must be M, and the sum of the 1y[] entries must be N.

MatSetValuesStencil

Inserts or adds a block of values into a matrix. Using structured grid indexing

Synopsis

#include "petscmat.h" PetscErrorCode MatSetValuesStencil(Mat mat,PetscInt m,const MatStencil idxm[],PetscInt n,const MatStencil idxn[],const PetscScalar v[],InsertMode addv) **Not Collective**

Input Parameters

- mat the matrix
- m number of rows being entered
- **idxm** grid coordinates (and component number when $dof > 1$) for matrix rows being entered
- number of columns being entered
- $idxn$ grid coordinates (and component number when dof > 1) for matrix columns being entered
- a logically two-dimensional array of values \mathbf{v}

addy-either ADD VALUES or INSERT VALUES, where ADD VALUES adds values to any existing entries, and INSERT VALUES replaces existing entries with new values

- We started from the automated matrix API available in PETSc
- Advantadges:
	- Automatic management of the local/global mapping.
	- To fill the matrix the user specify the local entries.
- Disadvantages:
	- Lack of control.

Test case: JT60-SA from turbulent restart

● Setup:

- System size: Nx=1200 Ny=2000 Nz=8
- Machine: single socket skylake with 20 cores plus V100
- Solver: DGMRES Preconditioner: Hypre/BoomerAMG
- 1 GBS step
- Goal: compare the performance of AMGX(GPU) vs PETSc(CPU)
- The AMGX options can be further tuned.
- It would be possible to use AmgXWrapper but it would not improve the matrix building.

KEY POINT: TO ACHIEVE MAXIMUM PERFORMANCES IS NECESSARY TO LOOK AT ALL THE ASPECTS

From DMDA to CSR

- AMGX uses the CSR format.
- PETSc has many options for debugging: -matview

- This tool helped to understand how to create the local/global mapping in CSR.
- To port the matrix building on GPU with CUDA we had to:
	- Create the matrix with AMGX.
	- Populate the matrix with CUDA kernel.
- ~20X faster wrt to CPU. Perhaps there is room for optimization in the CPU version.

Conclusion and perspective

- Lesson 1: automatism comes at a price, **performance**.
- Lesson 2: It is necessary to choose your evil.
	- Usually, libraries and compilers support C/C++ first.
		- Sometimes there is a native fortran binding (PETSc).
		- In other cases it has to be created (AMGX).
	- In principle the matrix building could have been done with CUDA Fortran, OpenACC or OpenMP. However, only GNU C/C++ is capable to compile AMGX.
	- The hardest part of the matrix building porting was the compatibility C/Fortran.
	- However, this part can be embedded into a library, so the application developers don't need to deal with C.
- The performance boost obtained in the matrix building is well promising for the RHS operations.

RHS computation

OpenMP Offload in GBS-RHS

- Goal: use GPUs in plasma evolution already used in Poisson/Ampere solver
- Use of OpenMP offload for Plasma subroutines

Neutrals updated every N plasma steps

OpenMP Offload for GPU

- CUDA only for NVIDIA GPU
- OpenMP offload for NVIDIA and AMD GPUs
	- Standardized, available for C, C++, and Fortran
	- Directive based multithreading library
	- Portable and ease of use, very good support (GNU, ARM, Intel, IBM, PGI, etc)
	- Less efficient than CUDA, high dependency on compilers
	- Performance of the classical stencil-based Jacobi example on SCITAS cluster: Xeon-Gold processors with 20 cores NVIDIA V100 GPUs (7TFLOPS)

OpenMP Offload in GBS-RHS

!Compute perpendicular gradients

• Example of OpenMP offloading in GBS:

subroutine perpendicular gradients use fields use array use gradients use time integration, only: updatetlevel use model.only:nlpol use prec const implicit none !Perpendicular gradients !\$omp target enter data map(alloc:strmfy,strmfx,pi y,pi x,thetay,thetax,tempey,strmfz,pi z) !somp target enter data map(alloc:theta curv op, tempe curv op, tempi curv op, strmf curv op, theta curv op v) ! \$omp task depend(in:strmf) call grady $n2n(strmf(:, :, :), strmfy(:, :, :))$ call gradx $n2n(\text{strmf}(:,:,:),\text{strmf}x(:,:,:))$ call gradz $n2n(\text{strmf}(:, \dots); \text{strmf}((:, \dots))$ call curv n2n(strmf(:,:,:), strmf curv op) !\$omp end task ! \$omp task depend(in:theta) call grady $n2n(theta(:,:,:,updatetlevel),thetay(:,:,:)))$ call gradx $n2n$ (theta(:,:,:,updatetlevel),thetax(:,:,:)) call curv n2n(theta(:,:,:,updatetlevel), theta curv op) call curv n2v(theta(:.:.:.updatetlevel).theta curv op v) ! \$omp end task ! \$omp task depend(in: tempe) call grady $n2n$ (tempe(:,:,:,updatetlevel),tempey(:,:,:)) call curv n2n(tempe(:,:,:,updatetlevel), tempe curv op) !\$omp end task ! \$omp task depend(in: pri) call grady $n2n(pri(:,:,:),pi y(:,:,:))$ call gradx $n2n(pri(:,:,:),pi x(:,:,:))$ call gradz $n2n(pri(:,:,:),pi[z(:,:,:))$! \$omp end task !\$omp target exit data map(from:strmfy,strmfx,pi y,pi x,thetay,thetax,tempey,strmfz,pi z) ! \$omp task depend(in: tempi) call curv n2n(tempi(:,:,:,updatetlevel), tempi curv op) ! \$omp end task !! \$omp target exit data map(from:theta curv op, tempe curv op, tempi curv op, strmf curv op, theta curv op v)

end subroutine perpendicular gradients

OpenMP Offload in GBS-RHS

Example of OpenMP offloading in GBS:

```
! parallel gradient for finite differences 4rth order from n grid to n grid
subroutine gradpar v2v fd4(f, flu, frd, f grad)
```

```
use prec const
```

```
implicit none
real(dp), dimension(iysq:iyeq,ixsq:ixeq,izsq:izeq), intent(in) :: f
real(dp), dimension(ivsg:iveg.ixsg:ixeg.izsg:izeg), intent(out): f grad
real(dp), dimension(iysq:iyeq,ixsq:ixeq,izsq:izeq) :: f z,f y,f x
real(dp), dimension(iylg:ny zg, ixsg: ixeg, 2), intent(in) :: flu, frd
integer :: ix, iy, iz: f grad(:,:,:) = nan
!$omp target enter data map(alloc:f z,f y,f x)
call gradz n2n fd4(f, f z)call grady n2n fd4(f, f y)
call gradx n2n fd4(f, f x)
! $omp target teams distribute parallel do simd collapse(3)
do iz = izs.ize
  do ix = ixs, ixe
      do iy = iys, iye
         f qrad(iy,ix,iz) = qradpar z*f z(iy,ix,iz) + qradpar y v(iy, ix)*f y(iy,ix,iz)&
              + qradpar x \vee (iy, ix) * f \times (iy, ix, iz)end do
  end do
end do
```

```
!$omp end target teams distribute parallel do simd
!$omp target exit data map(delete: f z, f y, f x)
```

```
end subroutine gradpar v2v fd4
```
OpenMP Offload in GBS-RHS for GPU

- We compared initial CPU serial implementation vs OpenMP one
- Setup: Reduced TCV at 0.9T, 2 timesteps
	- Turbulent mode
	- Nx = 600 , ny = 1000 , nz = 4
	- 1 node piz-daint@CSCS
		- 12-core Intel Xeon 64GB RAM
		- 1 NVIDIA Tesla P100 16GB
	- Cray Compiling Environment

OpenMP Offload in GBS-RHS for GPU

- We compared initial CPU serial implementation vs OpenMP one
- Setup: Reduced TCV at 0.9T, 2 timesteps
	- Turbulent mode
	- Nx = 1200 , ny = 2000 , nz = 4
	- 1 node piz-daint@CSCS
		- 12-core Intel Xeon 64GB RAM
		- 1 NVIDIA Tesla P100 16GB
	- Cray Compiling Environment

OpenMP offload in GBS

- Ongoing work:
	- asynchronous operations between CPU and GPU, identify kernels to be ported on GPU, overlap data transfer
	- To get more performance, test IBM xl compiler on MARCONI-100
	- Test new GCC 11.2 [\(2021-07-28\)](https://gcc.gnu.org/pipermail/gcc/2021-July/236903.html) fully supporting OpenMP offload: "*For Fortran, OpenMP 4.5 is now fully supported and OpenMP 5.0 support has been extended, including the following features which were before only available in C and C++"*
	- optimize CPU/GPU data transfer

OpenMP in GBS for CPU

- Each GPU is usually associated to a single MPI process
- How to exploit remaining cores :
	- associate a single core to a single MPI process (usually requiring collective MPI communications to transfer data to GPU)
	- use OpenMP to exploit remaining cores
	- use OpenMP from OpenMP-offload development is straightforward (compilation option)

OpenMP in GBS-RHS for CPU

- We compared initial CPU serial implementation, pure OpenMP one and pure MPI one
- Setup: Reduced TCV at 0.9T, 2 timesteps
	- Turbulent mode
	- Nx = 600 , ny = 1200 , nz = 4
	- 1 node izar
		- Xeon-Gold processors running at 2.1 GHz, with 20 cores each
		- Intel compiler

Plasma module: speed up for MPI and OpenMP versions (#OpenMPthreads=#cores and #MPIprocess=#cores)

Number of cores

- Goal: adapt the work done with OpenMP offload to use OpenACC: --> "replace" OpenMP directives by OpenACC directives for loop and data transfer:
	- first, using unified memory with OpenACC compiling with -acc -ta=tesla:managed
	- then optimize data transfer following current openmp offload data transfer

OpenACC in GBS

- Piz daint with PGI compiler
- bandwidth (Saxpy openacc test) = 474 GB/s
- theoritical peak 4,7 TFlops
- kernel compute bound if AI>9
- Kernels in RHS are memory bound
	- \circ kernel1: AI = 7/24 --> Memory bound
	- \circ kernel2: AI = 31/24 --> Memory bound

kernel1 subroutine gradz $n2n$ fd4(f, fz) use prec const **IMPLICIT** none real(dp), DIMENSION(iysg:iyeq,ixsg:ixeq,izsg:izeq), INTENT(in) :: f real(dp), DIMENSION(iysg:iyeg,ixsg:ixeg,izsg:izeg), intent(out) :: f z $integer :: iz$ real(dp), DIMENSION(1:4) :: coef der $coef \, der(:) = deltazi*coef \, derl n2n(:)$ \pm f z(:,:,:) = nan do iz=izs, ize $f_z(:, :, iz) =$ coef_der(1)*f(:, :, iz-2) & + coef der(2)*f(:, :, iz-1) & + coef der(3)*f(:, :, iz+1) & + coef $der(4)*f$ (:, :, iz+2) end do end subroutine gradz n2n fd4

kernel2

```
subroutine gradz v2n fd4(f,f z v2n)
 use prec const
 real(dp), DIMENSION(iysg:iyeg,ixsg:ixeg,izsg:izeg), INTENT(in) :: f
 real(dp), DIMENSION(iysg:iyeg,ixsg:ixeg,izsg:izeg), intent(out) :: f z v2n
 integer :: iy, iz
 real(dp), DIMENSION(1:4) :: coef der
 coef \, der(:) = deltazi*coef \, der1 staq(:)\pm f z v2n(:,:,:) = nan
 do iy=iys, iye
     do iz=izs, ize
        f z v2n(iy,:,iz) = coef int(1)*( coef der(1)*f(iy-1, :, iz-1) &
             + coef der(2)*f(iy-1, : iz)\delta+ coef der(3)*f(iy-1, :, iz +1) &
             + coef der(4)*f(iy-1, :, iz+2) )\&+ coef int(2)* ( coef der(1)*f(iy, :, iz-1)
                                                                 \mathcal{S}_{\mathbf{r}}+ coef der(2)*f(iy, \ldots, iz)+ coef \, der(3)*f(iy, \ldots 1Z+1)\delta+ coef^-der(4) * f(iy, : , iz+2)\delta+ coef int(3)*( coef der(1)*f(iy+1, :, iz-1) &
             + coef der(2)*f(iy+1, :, iz)+ coef der(3)*f(iv+1. :. iz+1)
                                                ୍ଷ
             + coef der(4)*f(iy+1, :, iz+2) ) &
             + coef int(4)^{*} ( coef der(1)*f(iy+2, :, iz-1) &
             + coef der(2)*f(iy+2, : , iz)+ coef der(3)*f(iy+2, : , iz+1)\delta+ \text{ coeff der}(4) * f(iv+2, : iz+2)end do
 end do
end subroutine gradz v2n fd4
```
- We compared initial CPU serial implementation vs OpenACC one
- Setup: Reduced TCV at 0.9T, 2 timesteps
	- Turbulent mode
	- Nx = 600 , ny = 1200 , nz = 4
	- 1 node piz-daint@CSCS
		- 1 NVIDIA Tesla P100 16GB
	- PGI Compiling Environment

- Conclusion:
	- Compared to cpu (one core) version, we observed a speed up x2 for the Unified Memory OpenACC version and a speed up x4 for the OpenACC version managing data transfer
	- Memory peak usage: 10GB
- In progress:
	- optimize data transfer
	- use multiple GPU
	- Test new GNU 11.2 compiler supporting OpenACC

- **Nsys profiling**
	- Multiple streams version using *async/wait* directives

