Introduction to radiation effects in electronics (and detectors)

8th EIROforum School on Instrumentation

2024/05/14 – ESO/EUROfusion Garching (Germany)

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CERN

radiation effects in electronics:

any radiation/electronic device interaction that can perceptibly influence the expected behavior of the electronic device

RADIATION EFFECTS	IONIZING	NON-IONIZING
CUMULATIVE	TOTAL IONIZING DOSE (TID)	DISPLACEMENT DAMAGE
STOCHASTIC	SINGLE EVENT EFFECTS	------------------------

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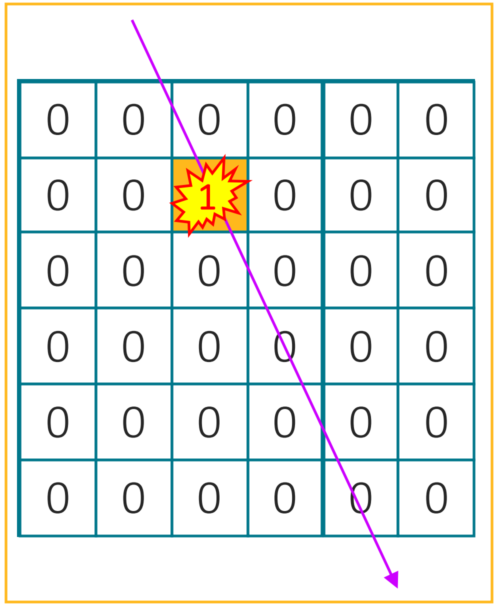
what are SEE effects?

Single Event Effects (SEEs) are any measurable disturbance on a circuit resulting from a **single**, energetic particle strike

example:
an energetic particle flips a bit in a memory



Qantas Flight 72

… an inflight accident that included a pair of **sudden, uncommanded pitch-down manoeuvres** that caused severe injuries—including fractures, lacerations and spinal injuries

…

Unrestrained (and even some restrained) passengers and crew were flung around the cabin or crushed by overhead luggage, as well as crashing with and through overhead-compartment doors.

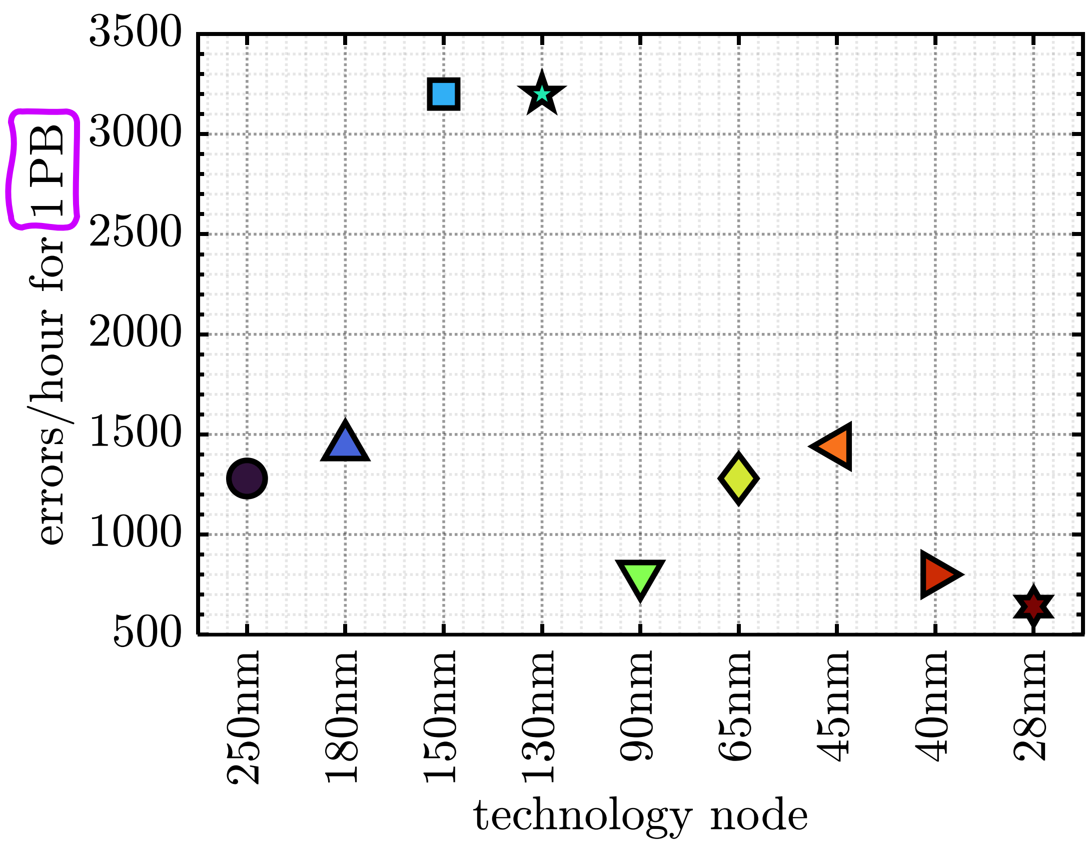
https://en.wikipedia.org/wiki/Qantas_Flight_72

https://www.youtube.com/watch?app=desktop&v=HKJ1lIh2Cgk&ab_channel=TheFlightChannel

Table 2: Typical Popular SRAM FPGA Configuration Upsets at Sea-Level in FIT/Mb (Failures in Time per Billion hours per Megabit of Configuration Memory)

Technology Node	FIT/Mb
250 nm	160
180 nm	180
150 nm	400
130 nm	400
90 nm	100
65 nm	160
45 nm	180
40 nm	100
28 nm	80

Microsemi: Single Event Effects - A Comparison of Configuration Upsets and Data Upsets
https://www.microsemi.com/document-portal/doc_view/135837-wp0203-single-event-effects-a-comparison-of-configuration-upsets-and-data-upsets



~1h course on SEE on Neural Networks

Experimental Evaluation of Artificial Neural Networks Reliability: from GPUs to low-power accelerators

Paolo Rech, *Senior Member, IEEE*
Università di Trento, Italy and Universidade Federal do Rio Grande do Sul, Brasil

How An Ionizing Particle From Outer Space Helped A Mario Speedrunner Save Time

Super Mario 64 speedrunner DOTA_Teabag received some cosmic help from an ionizing particle, resulting in an impossible glitch.

BY **MALCOLM DONALD** PUBLISHED SEP 16, 2020

Mario, Peach and Toad In Front Of Space

https://www.thegamer.com/how-ionizing-particle-outer-space-helped-super-mario-64-speedrunner-save-time/

RADIATION EFFECTS	IONIZING	NON-IONIZING
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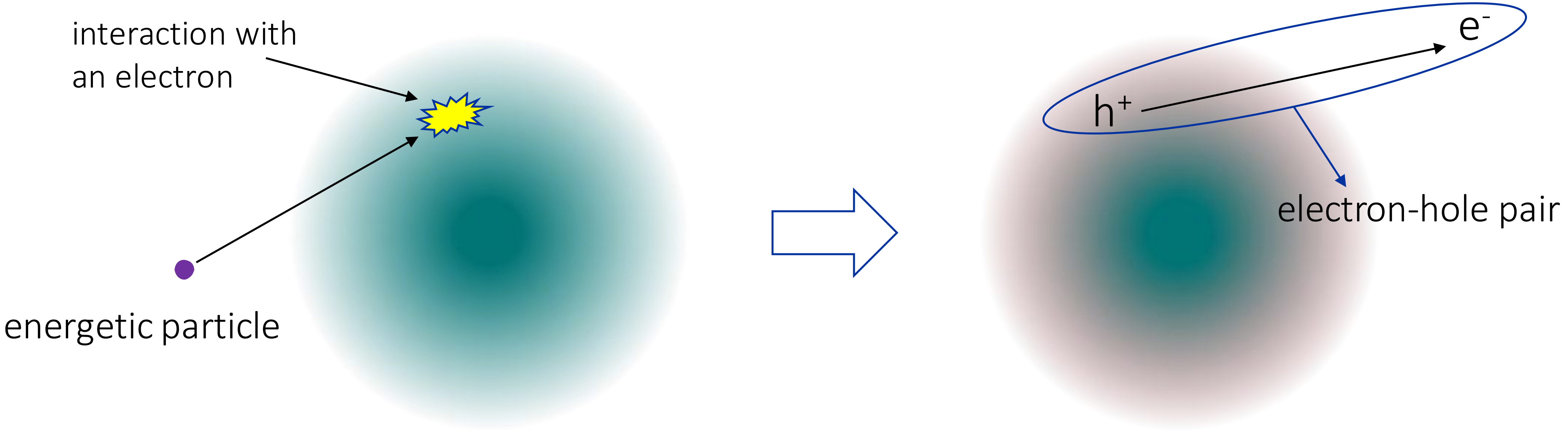
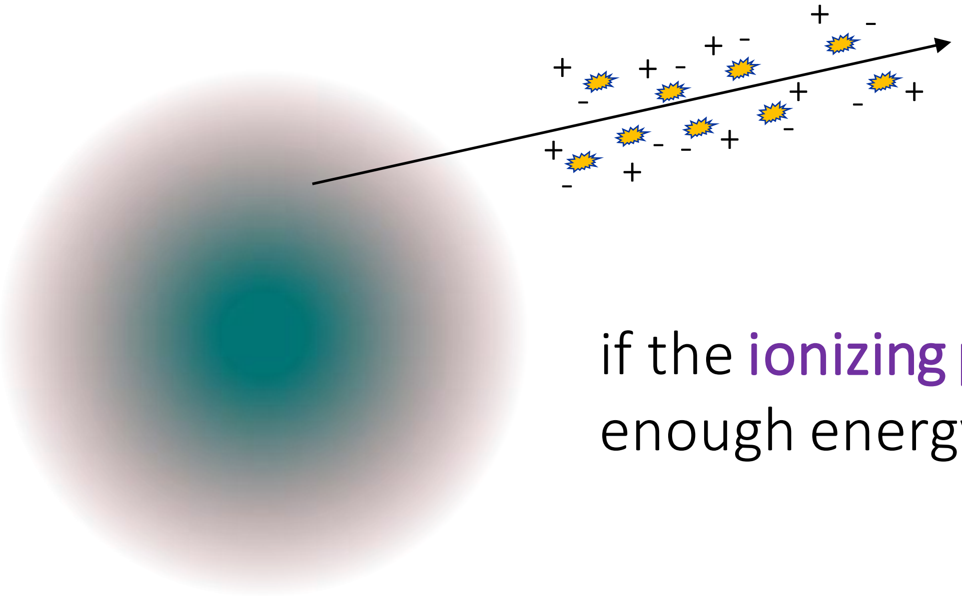
IONIZATION

neutral atom or molecule

charged atom or molecule





if the ionizing particle and/or the emitted electron have enough energy, they can ionize other atoms along their path

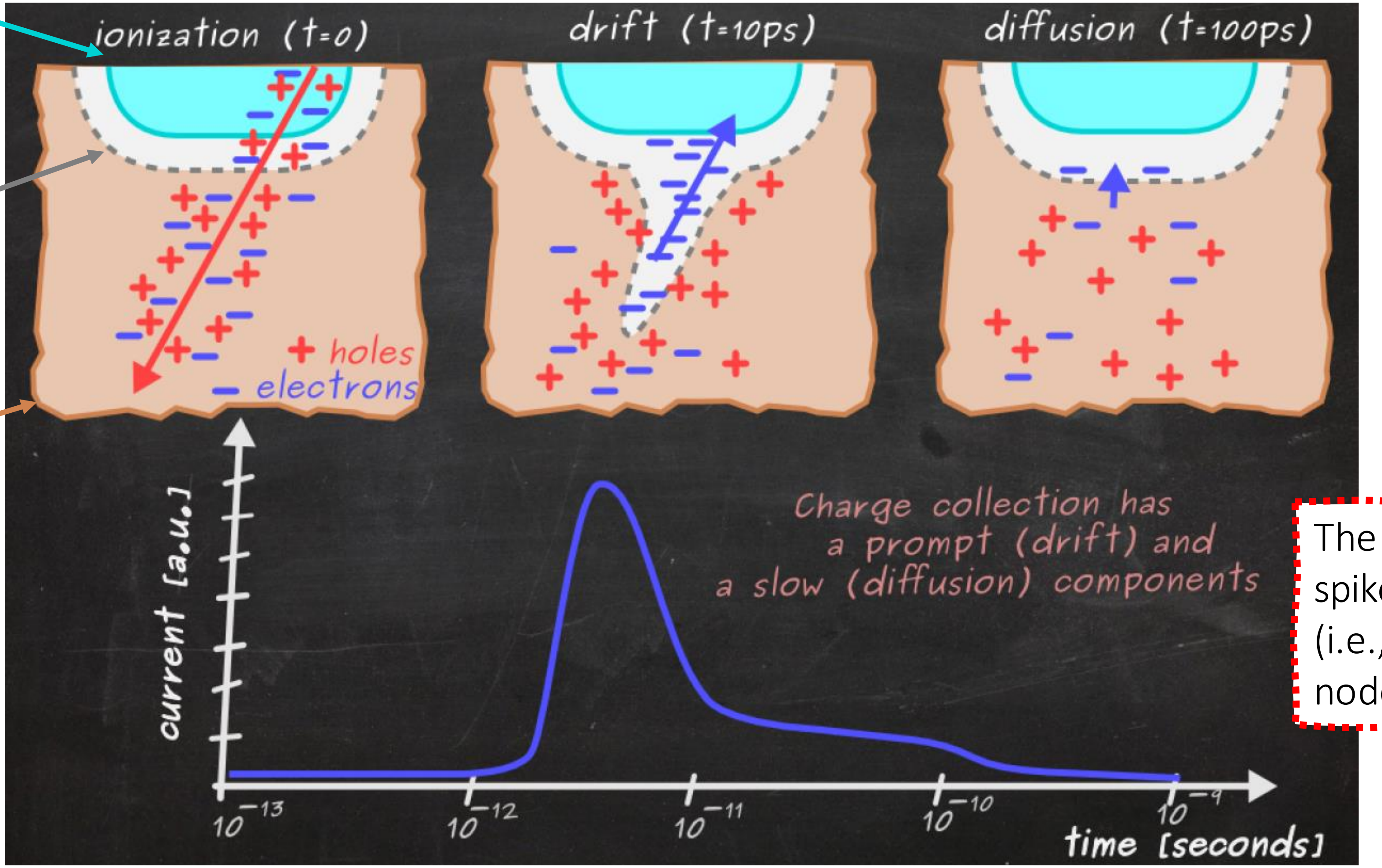
multiple electron-hole pairs

what are SEE effects?

n-doped Si
(V > 0)

depletion region

p-doped Si
(V = 0)



https://tmrg.web.cern.ch/tmrg/tmrg_kulis_in2p3.pdf

The effect of the current spike depends on where (i.e., in which circuit, cell, node, etc.) it occurred

Single Event Effects

non-destructive

- Single/Multi Event Upset
- Single Event Transient
- etc…

destructive

- Single Event Latch-Up
  (potentially destructive)
- Single Event Burn-out
- Single Event Gate Rupture
- etc…

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  (potentially destructive)
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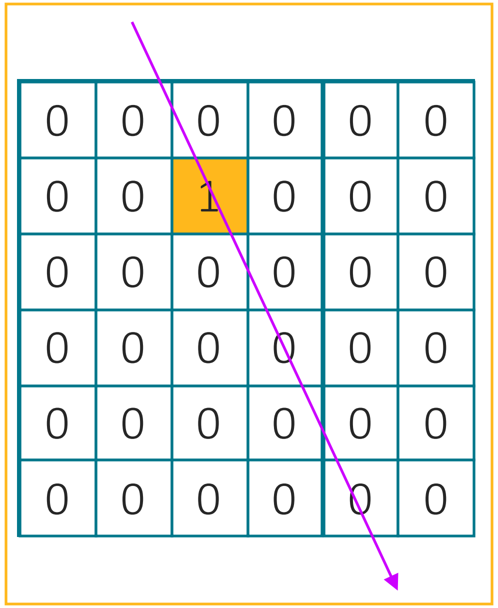
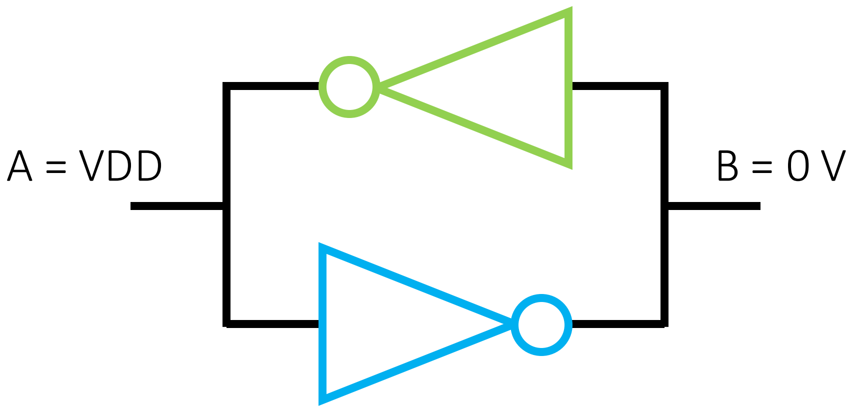
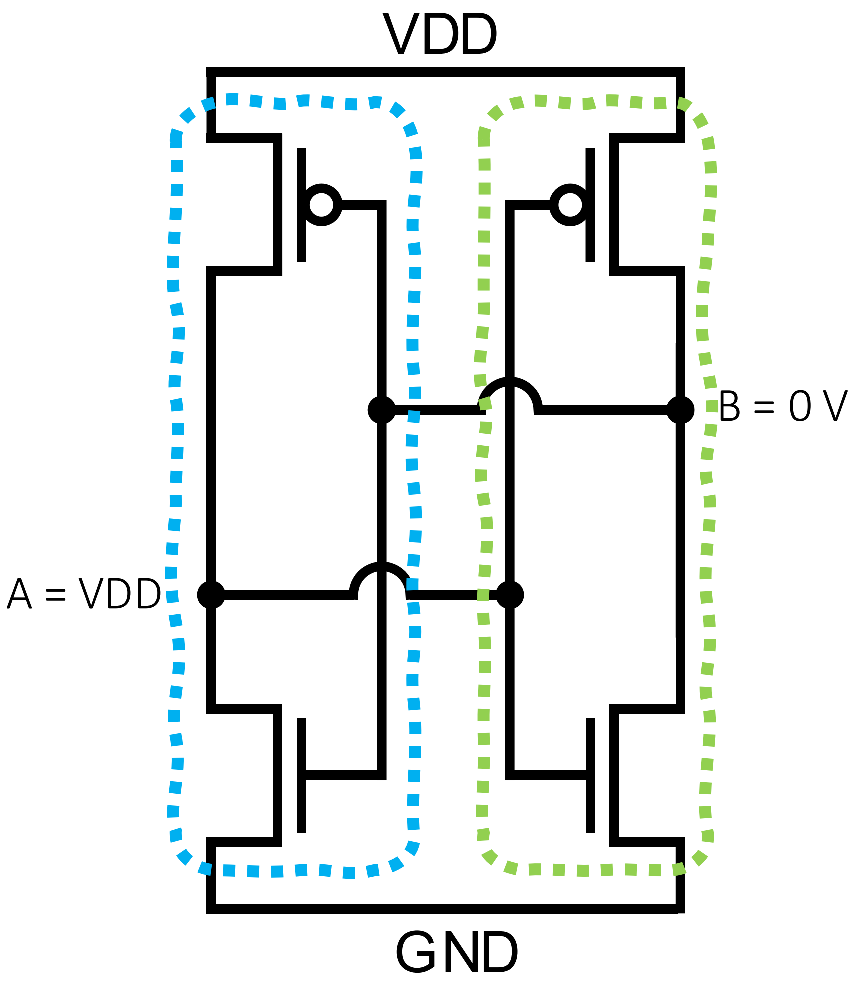
BIT-UPSET = change in the value of a bit caused by a particle

Single-bit-upset (SBU)

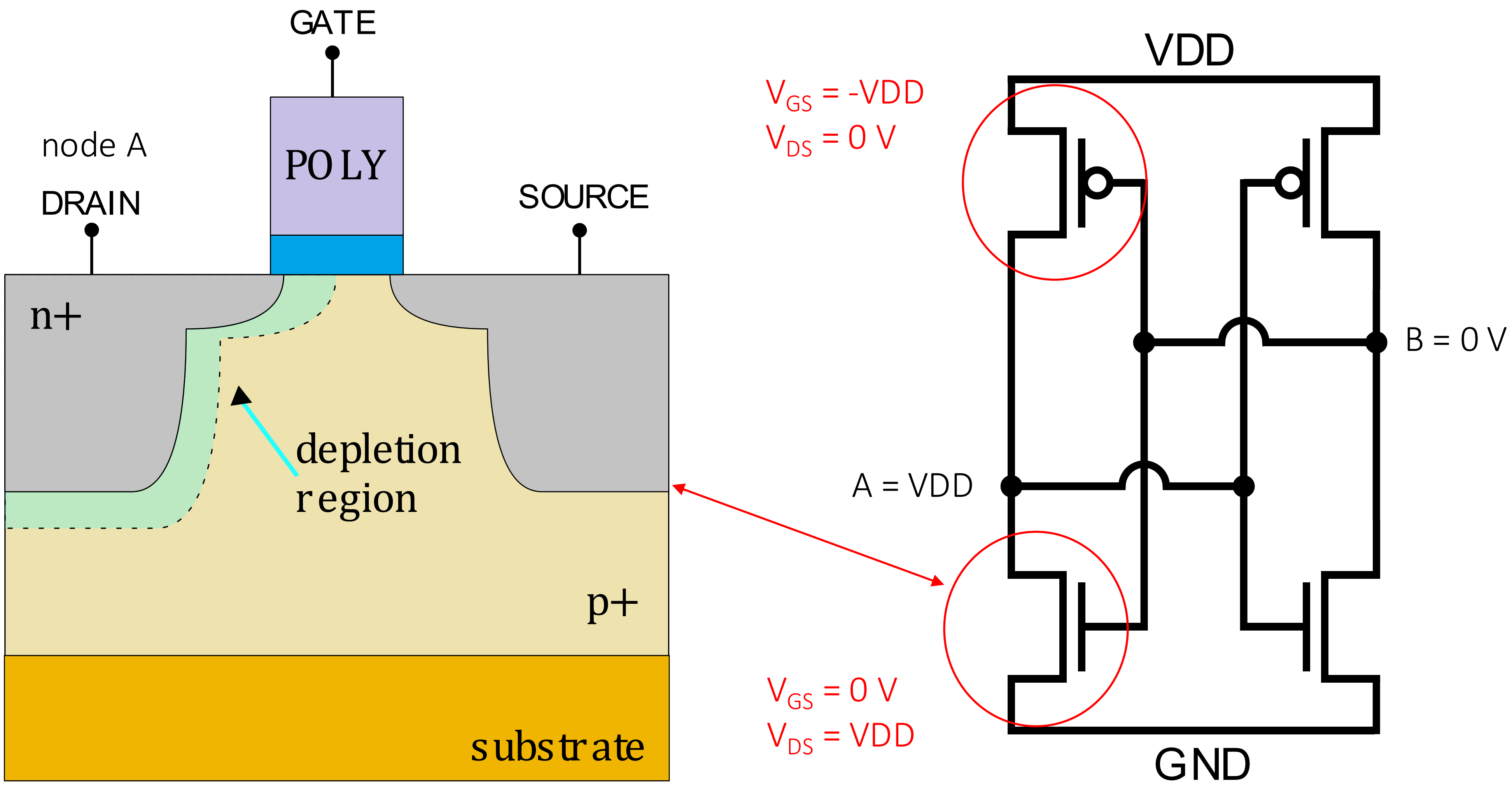


example: SRAM cell

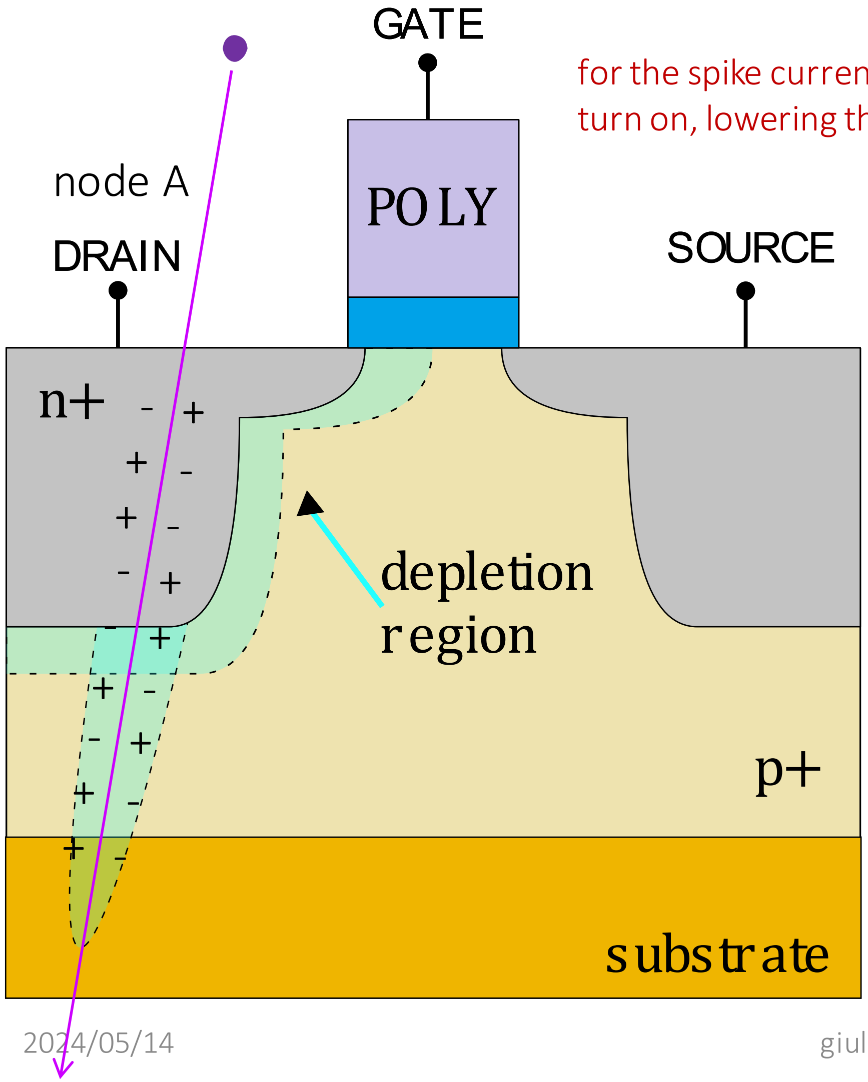




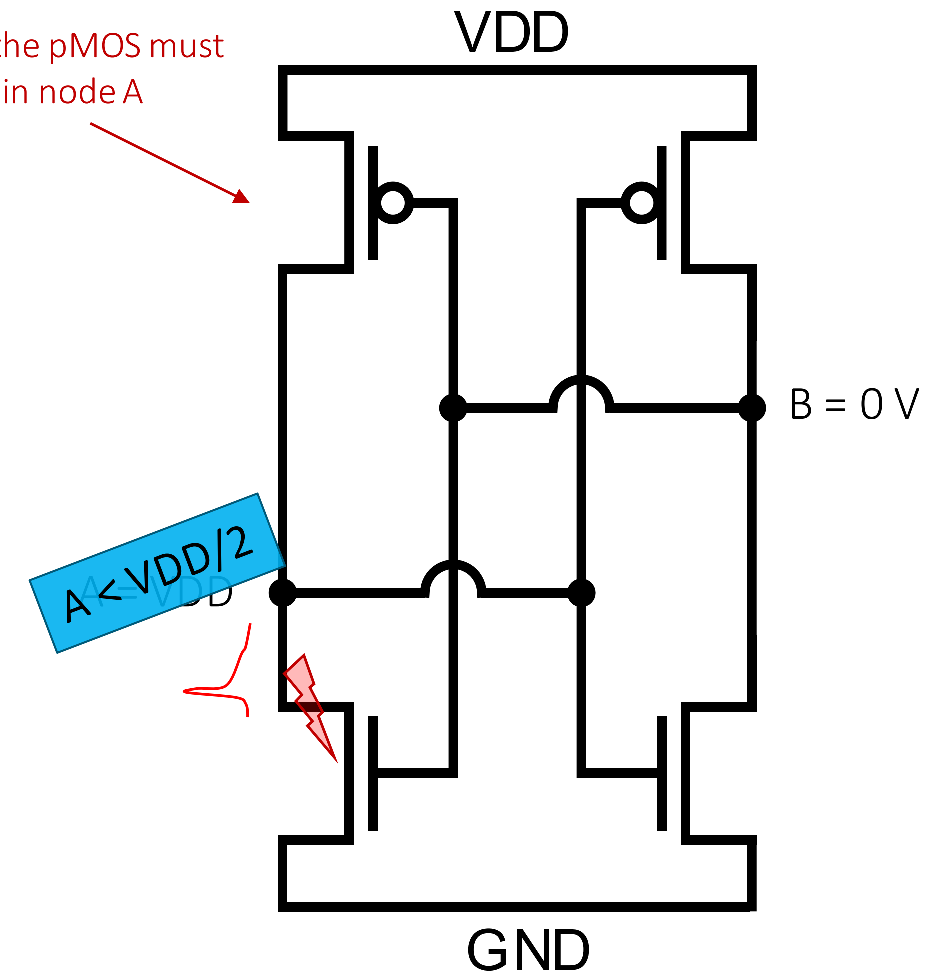
example: SRAM cell



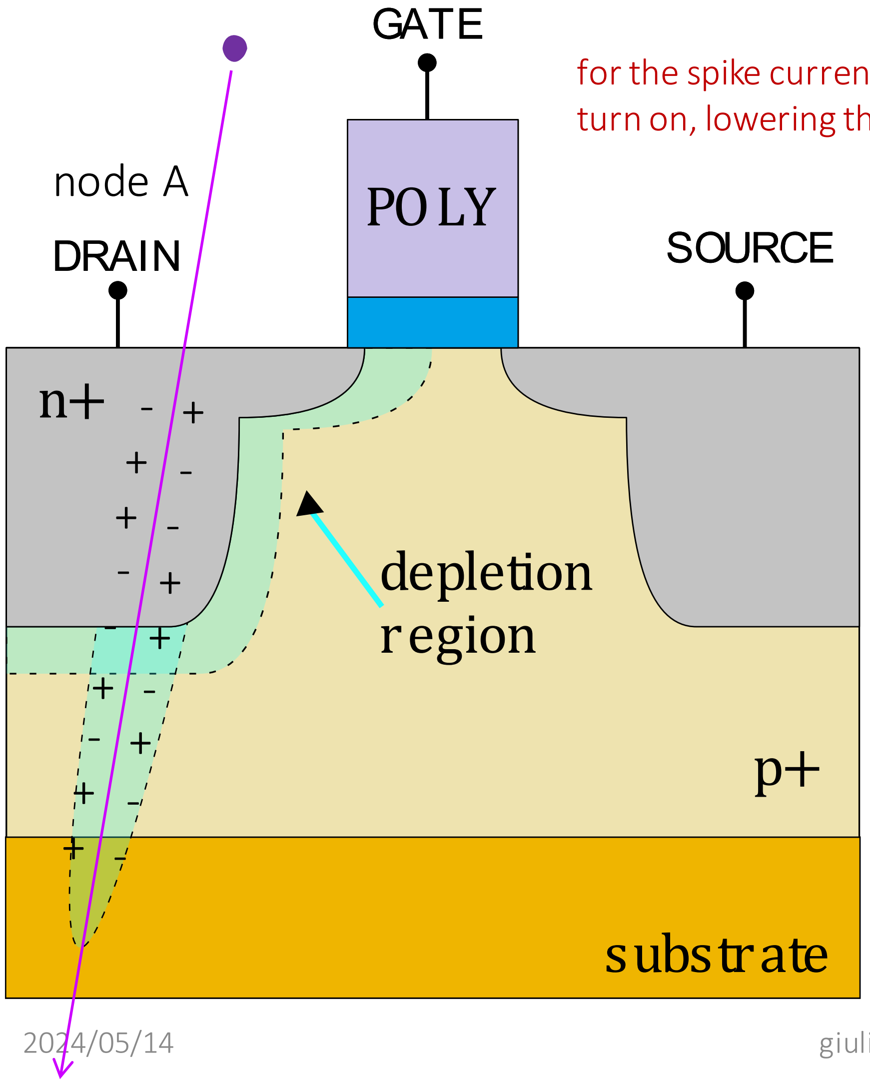
example: SRAM cell



for the spike current to flow, the pMOS must turn on, lowering the voltage in node A

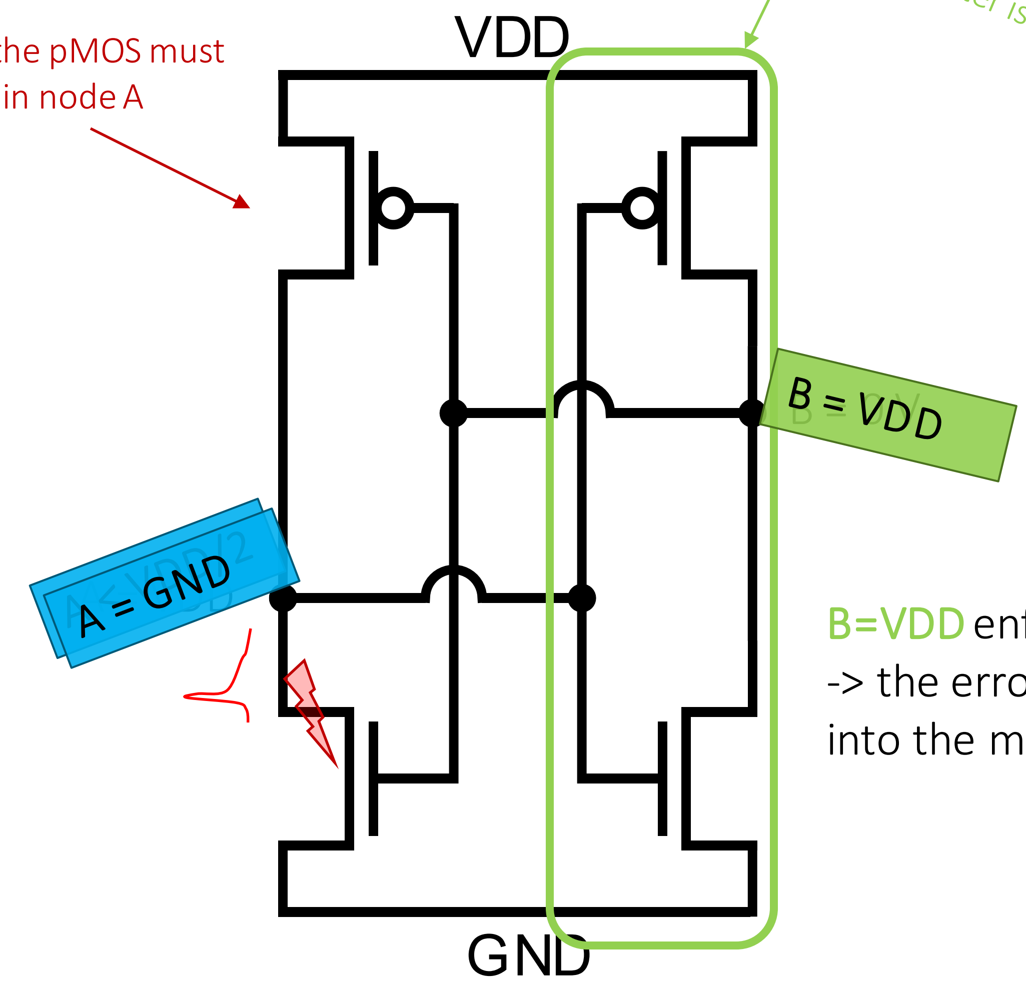


example: SRAM cell



for the spike current to flow, the pMOS must turn on, lowering the voltage in node A

now the input of this inverter is low enough
-> B = VDD



B=VDD enforces A=GND
-> the error is latched into the memory cell!

Single Event Effects

non-destructive

- Single/Multi Event Upset
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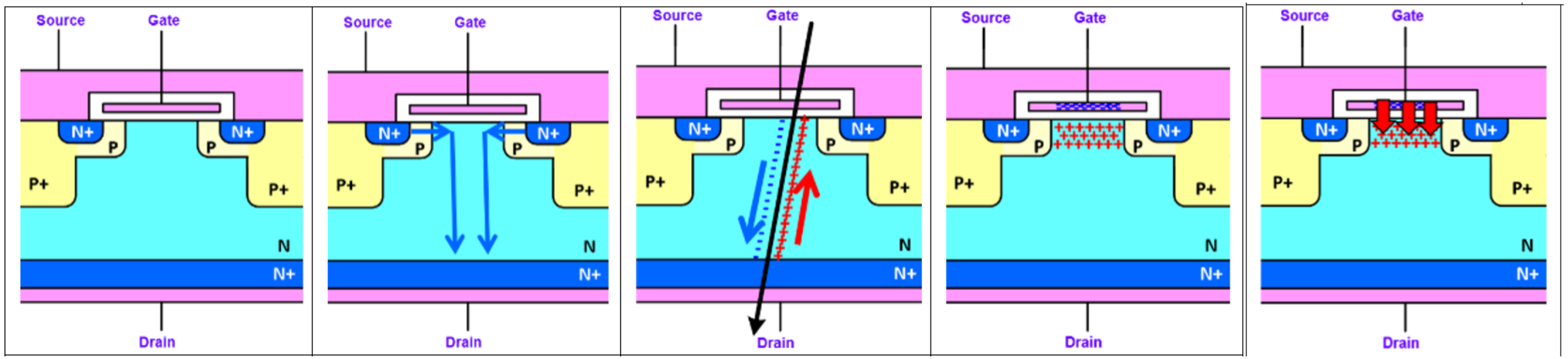
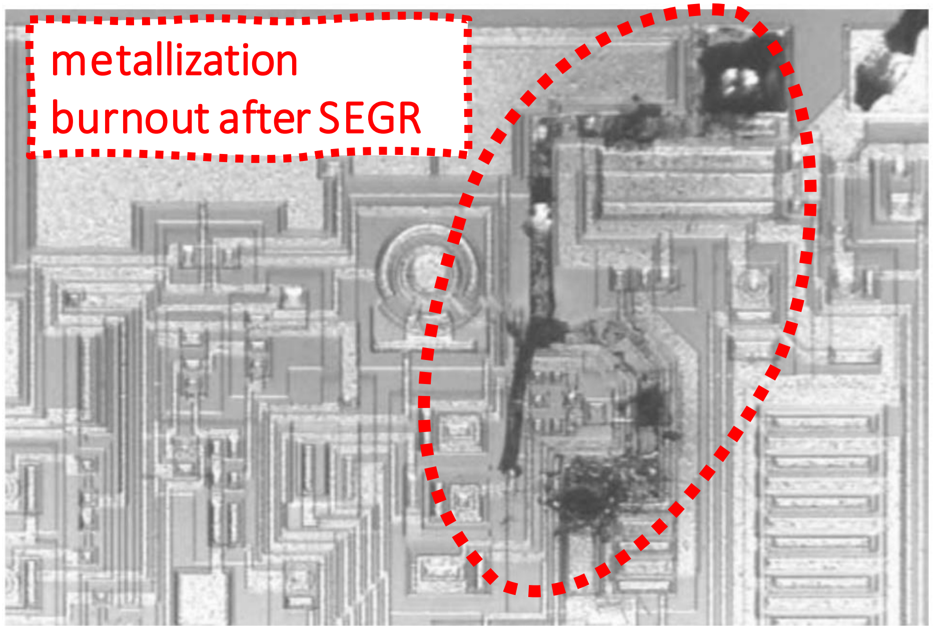
- etc…

destructive

- Single Event Latch-Up
  (potentially destructive)
- Single Event Burn-out
- Single Event Gate Rupture
- etc…

SEGR in power MOSFETs





G. K. Lum et al., "New experimental findings for single-event gate rupture in MOS capacitors and linear devices," in IEEE Transactions on Nuclear Science, vol. 51, no. 6, pp. 3263-3269, Dec. 2004, doi: 10.1109/TNS.2004.840262.

(a) Schematic view of power MOSFET cross section.
(b) ON mode. Current flows from source to drain. No electrical field in N/N+ drain junction.
(c) OFF mode. An ionized track crosses the structure. High electrical field in N/N+ drain junction separates its (+) and (-) charges.
(d) The (+) charges accumulate below gate oxide, and image (-) charges accumulate above gate oxide.
(e) This causes a high electrical field through the gate oxide, which causes a gate rupture.

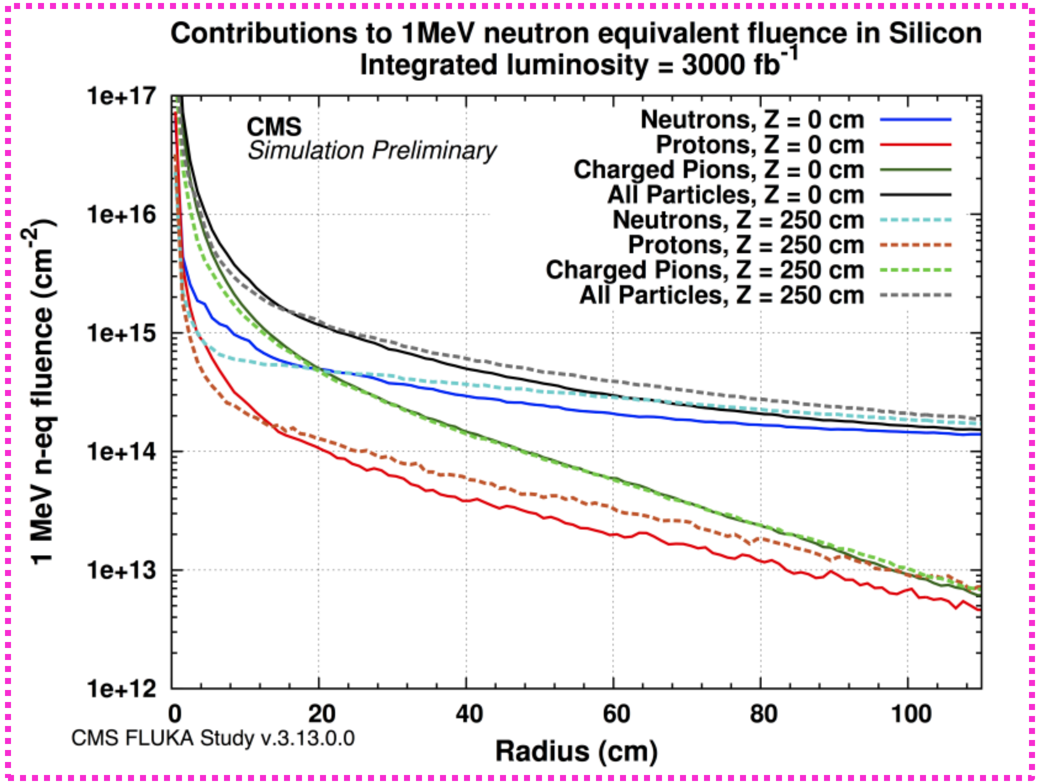
thanks Martin DENTAN for the slide!

How different particles ionize the material?

(from the point of view of radiation effects in electronics)

Different applications have different radiation environments!

CMS



W. Adam et al 2017 JINST 12 P06018, DOI 10.1088/1748-0221/12/06/P06018

SPACE

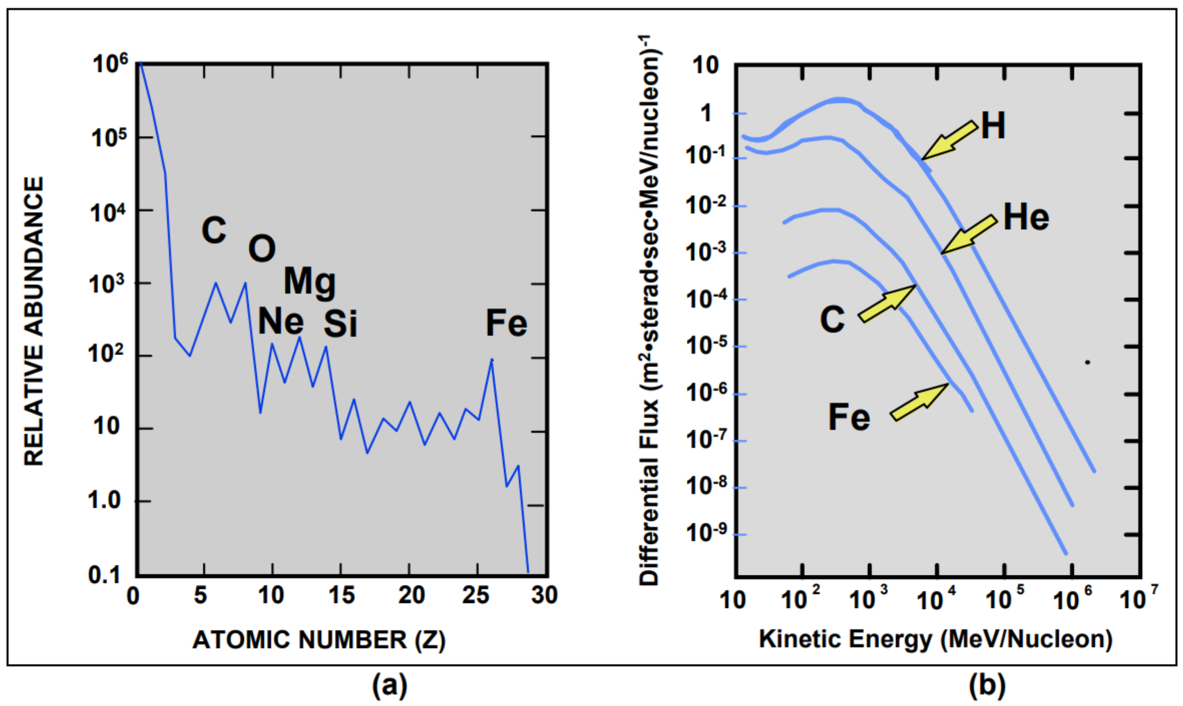
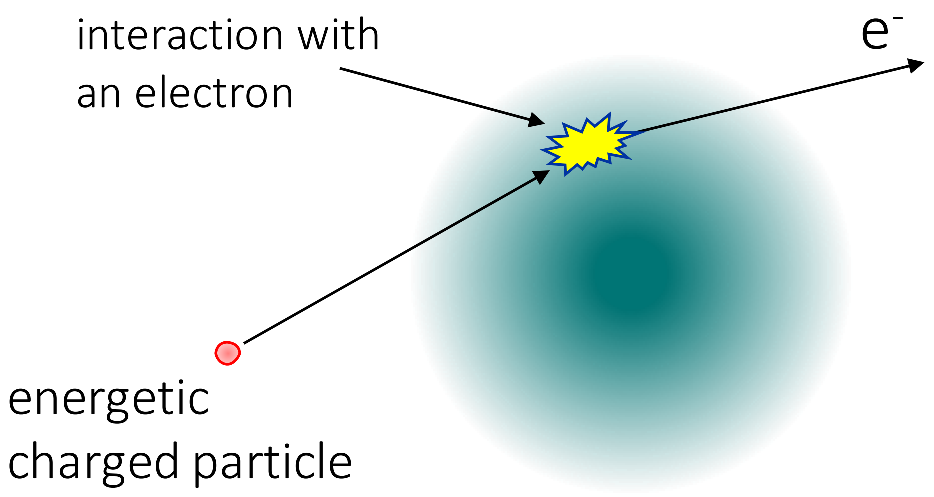


Figure D. 1. Abundances (a) and energy spectra (b) of GCR.

https://three.jsc.nasa.gov/concepts/SpaceRadiationEnviron.pdf

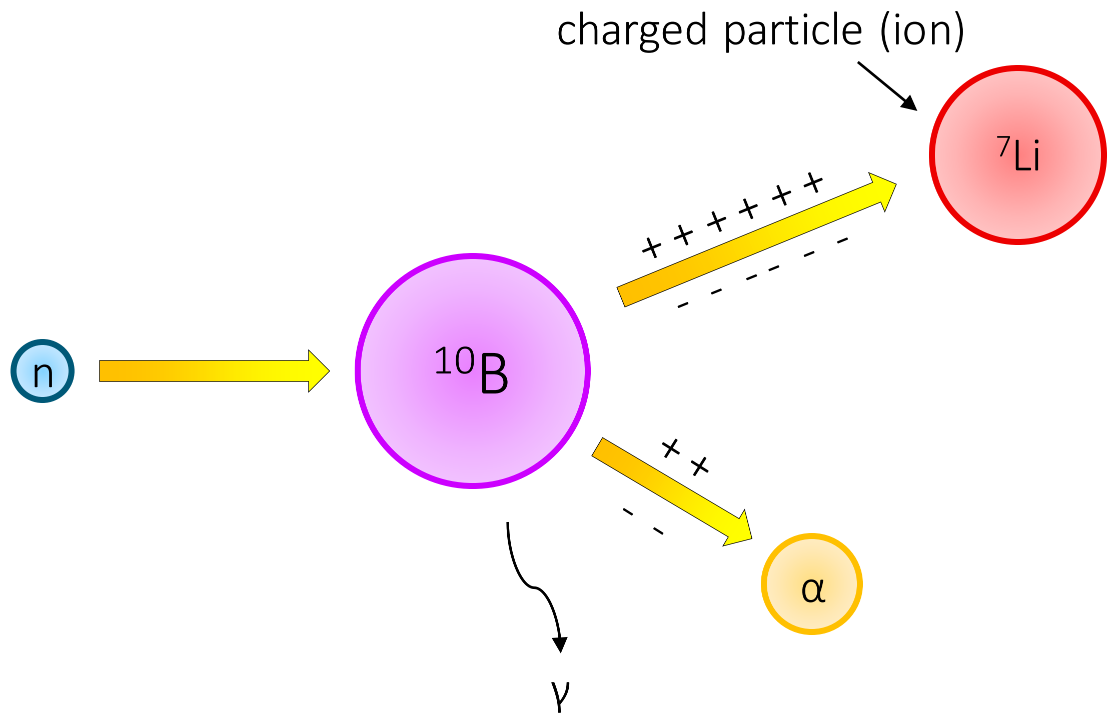
neutron flux at sea level: ~ 18 neutrons/cm2-hour with E>2 MeV
https://www1.lnl.infn.it/~lnldir/Seminario%20sorgenti/PDF/Wyss.pdf

direct ionization

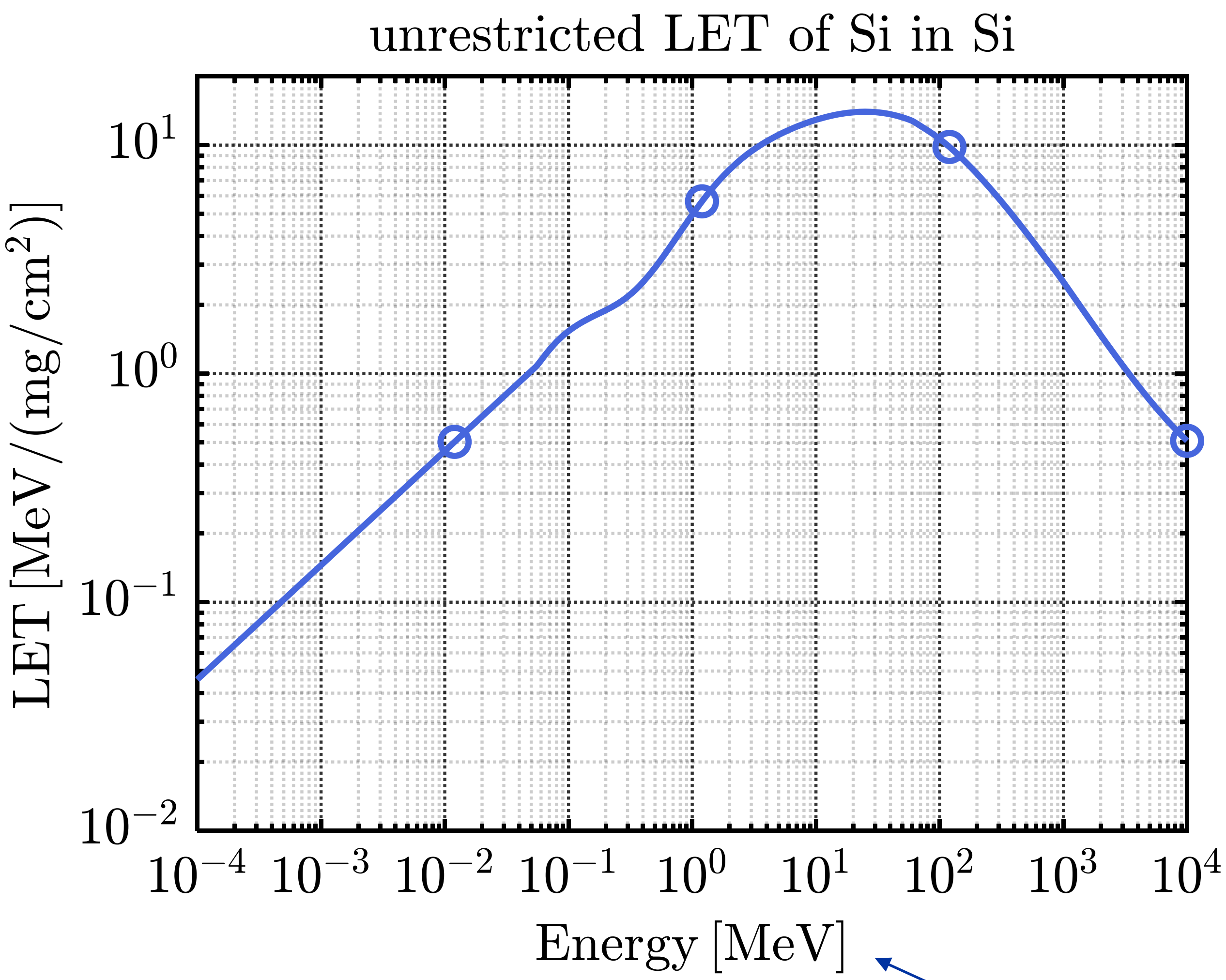


indirect ionization

all particles!



direct ionization

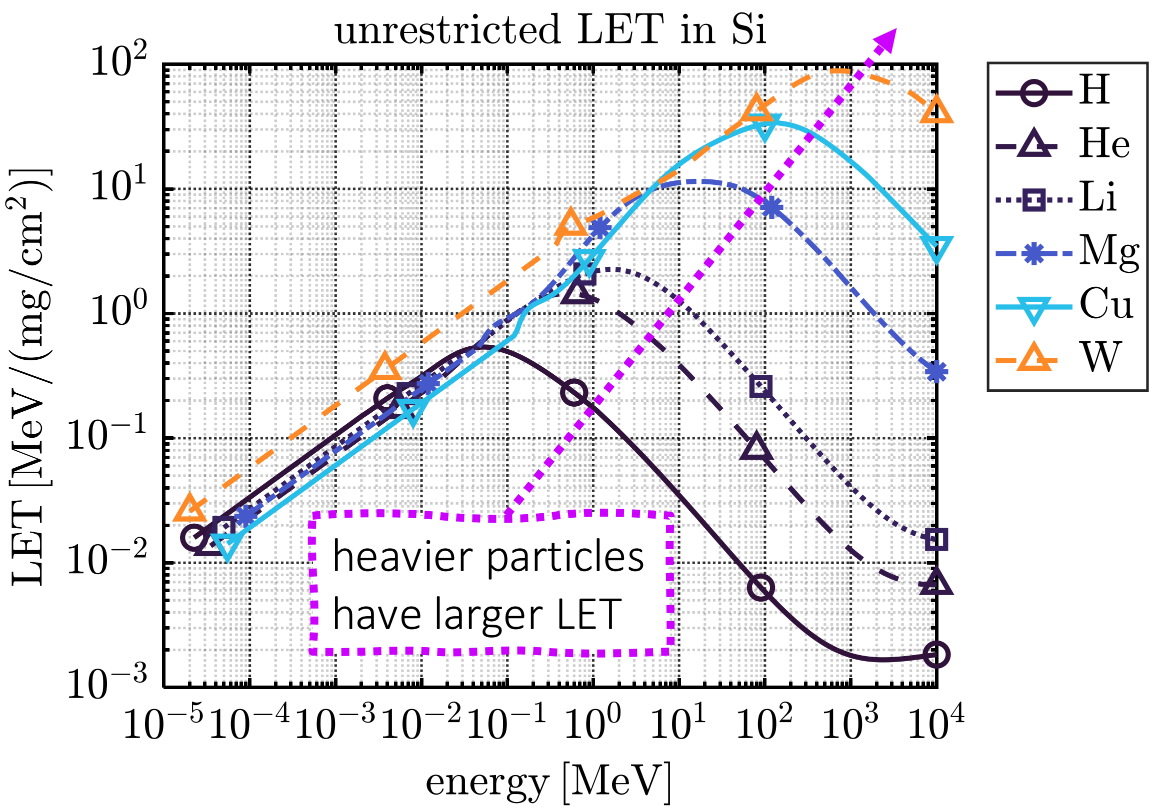


energy of incident particle

Calculated as electrical stopping power from SRIM tables:
J.F. Ziegler and J.P. Biersack, "Stopping and range of ions in matter," http://www.srim.org

The amount of energy per unit length "used" to directly ionize the material is called linear energy transfer (LET)

- $LET \cong -\frac{1}{\rho}\frac{\mathrm{d}E}{\mathrm{d}x} \left[\frac{\mathrm{MeV}}{(\mathrm{mg/cm^2})}\right]$



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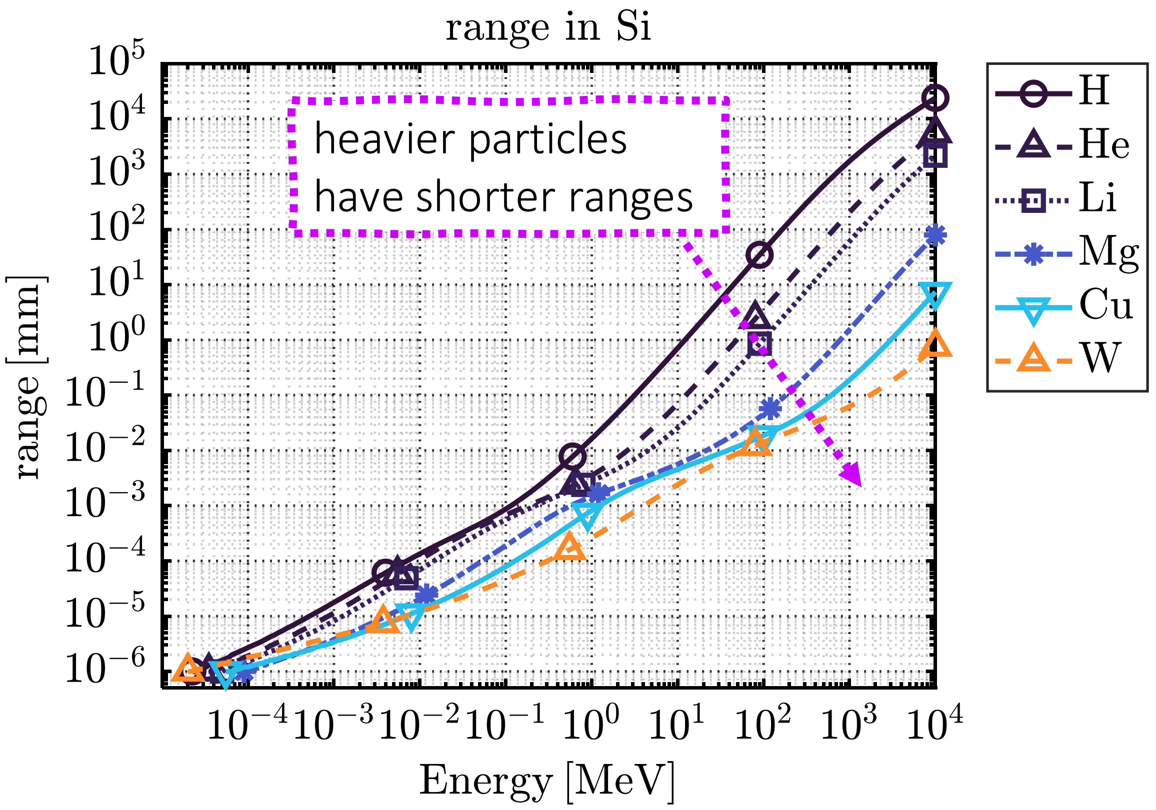
J.F. Ziegler and J.P. Biersack, "Stopping and range of ions in matter," http://www.srim.org



Calculated from electrical stopping power from SRIM tables:
J.F. Ziegler and J.P. Biersack, "Stopping and range of ions in matter," http://www.srim.org

For indirect ionizing interactions, we need to know the probability of an interaction event occurring.

example: neutrons

Different reactions have different probabilities (cross sections)

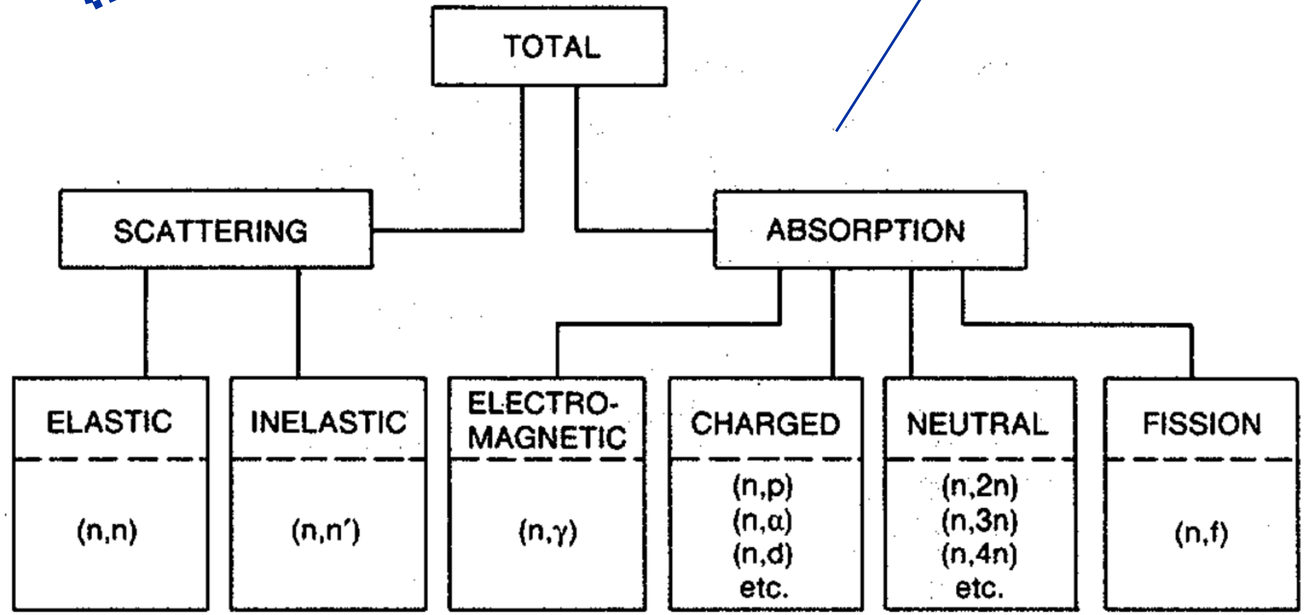
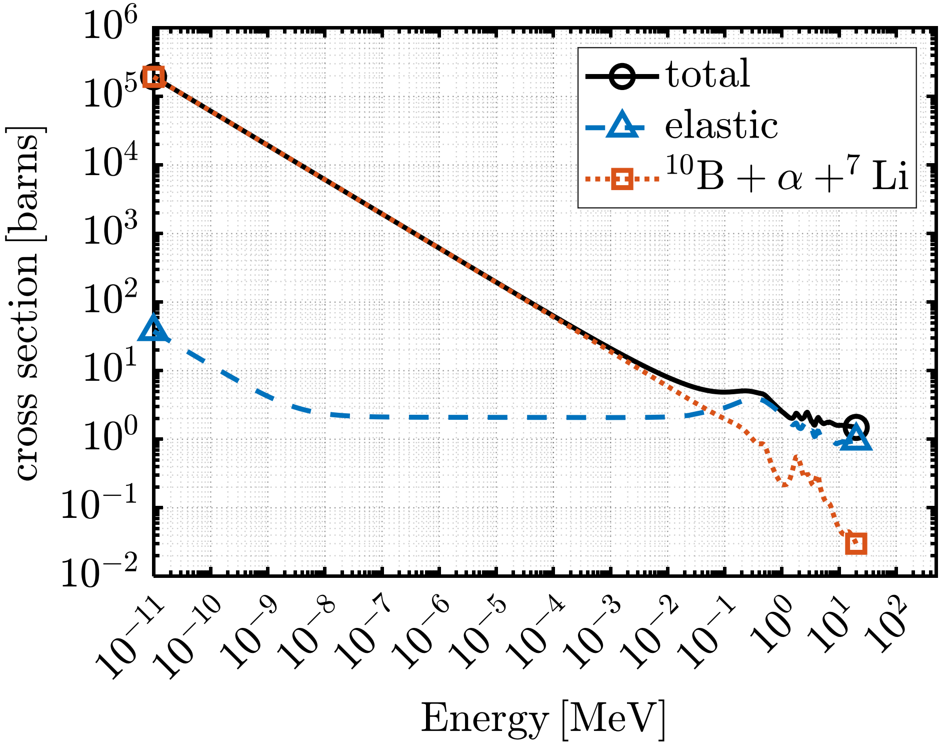
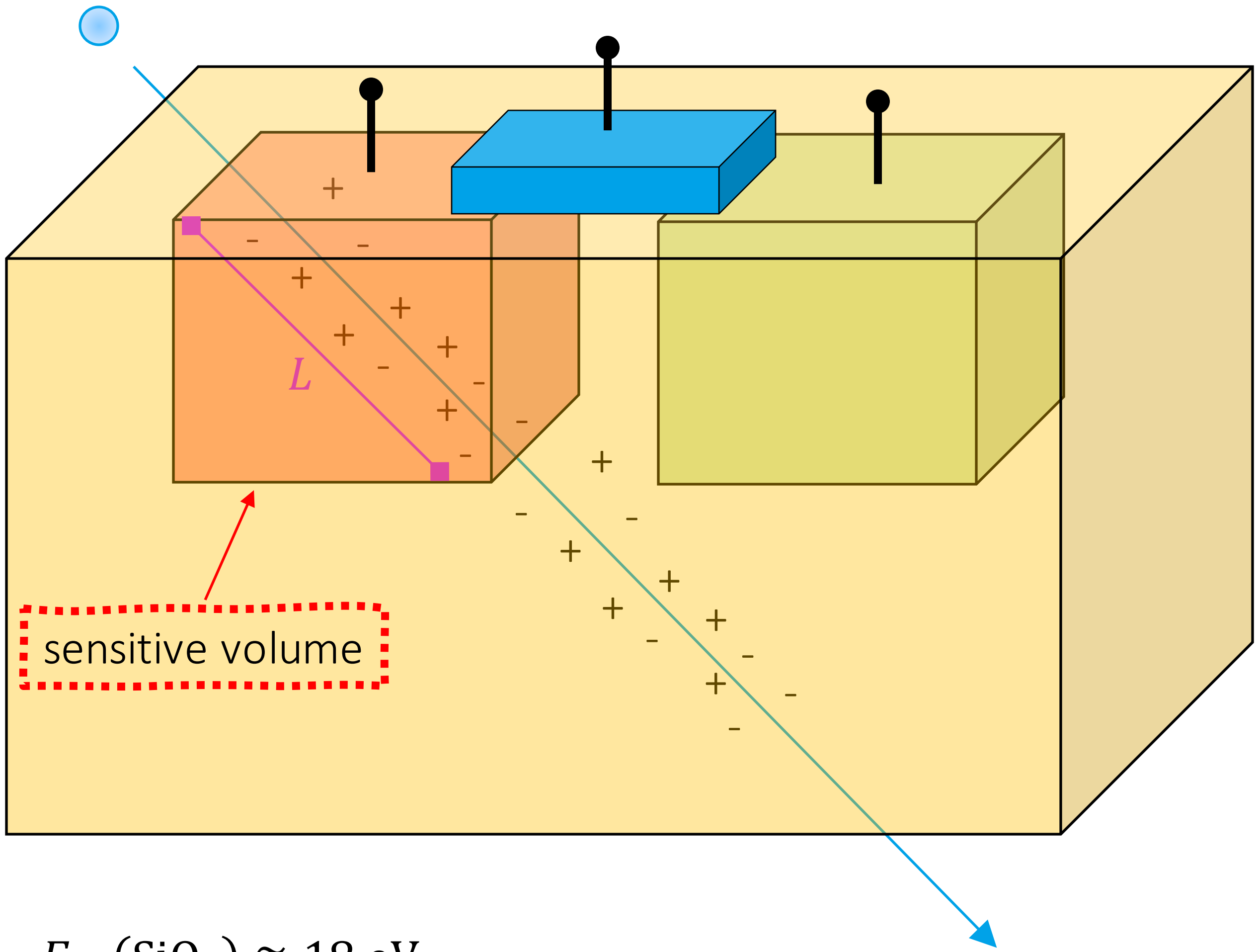


Figure: J.L. Autran, D. Munteanu, "Soft Errors, from Particles to Circuits",
Available at: http://www.fas.org/sgp/othergov/doe/lanl/lib-www/la-pubs/00326407.pdf)



Data from: https://www.nndc.bnl.gov/endf/
Database ENDF/B-VIII.0

energy needed to create an *e-h* pair in Si $E_{eh}(\mathrm{Si}) \cong 3.6\ \mathrm{eV}$



$$eh_{Si} = \frac{\int_0^L \rho_{Si} \times LET(E)\mathrm{d}x}{3.6\ \mathrm{eV}}$$

An upset is triggered if enough charge (critical charge) is deposited in the sensitive volume.

$E_{eh}(\mathrm{SiO_2}) \cong 18\ \mathrm{eV}$
$E_{eh}(\mathrm{Ge}) \cong 2.9\ \mathrm{eV}$

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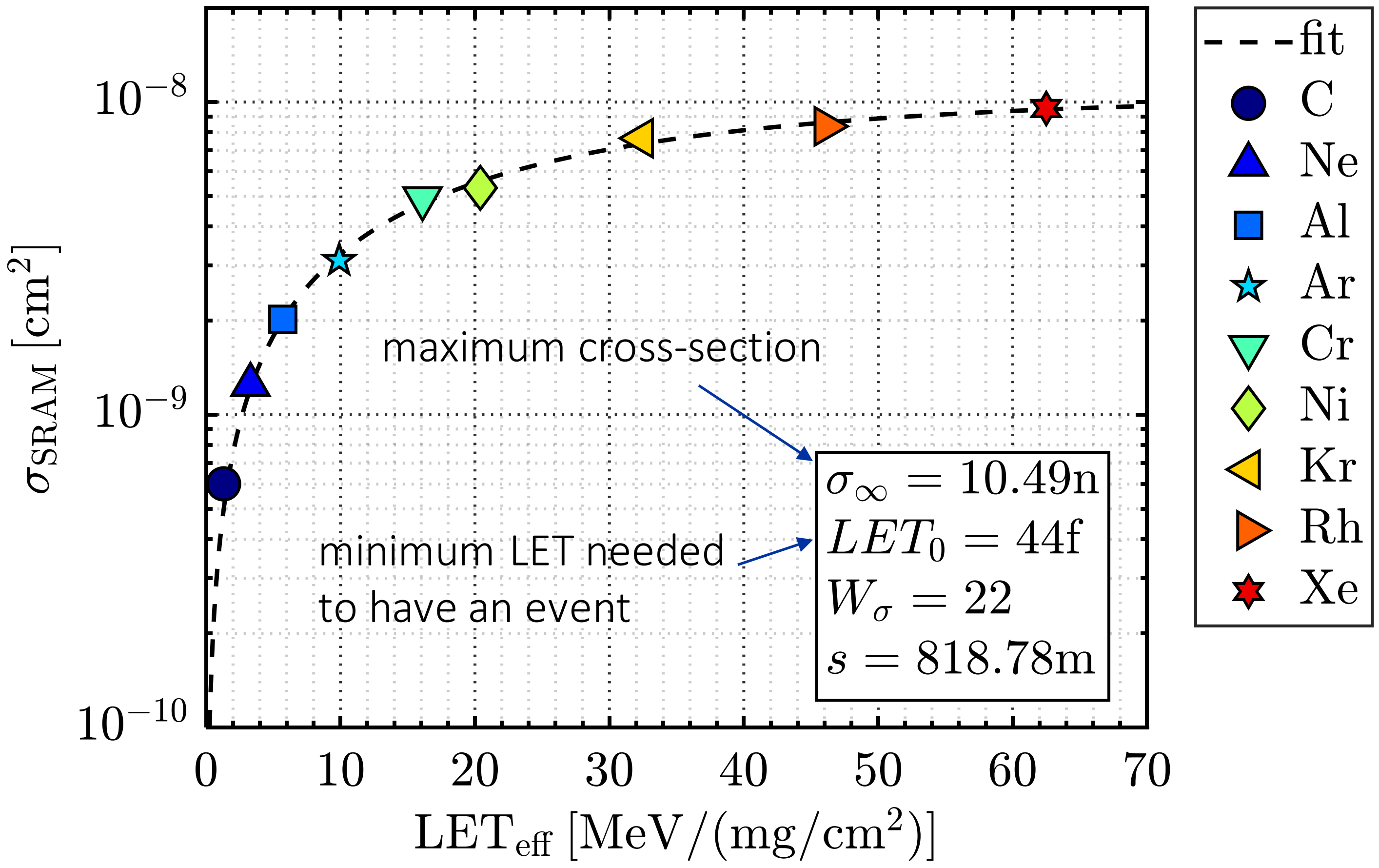
SEE are stochastic in nature

- a particle may or may not produce an error

SEE cross-section (σ) measures the probability for an SEE to occur

$$\sigma[\mathrm{cm}^2] = \frac{\text{number of errors}}{\text{fluence [particles/cm}^2]}$$

example: SRAM in 28nm CMOS technology

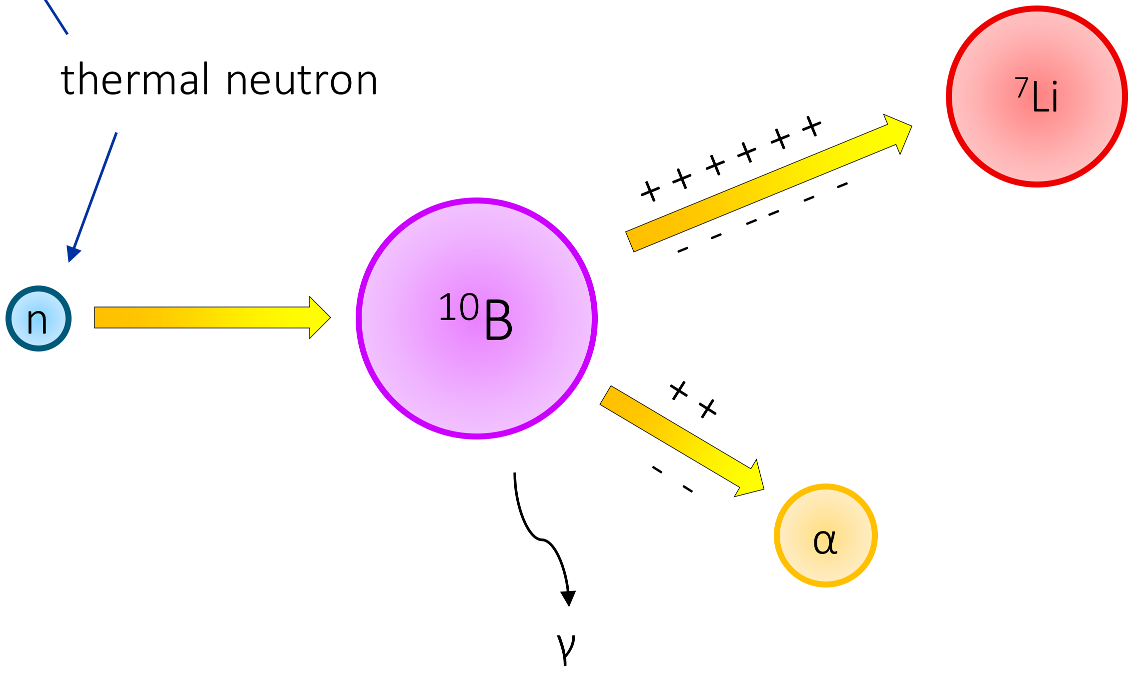


G. Borghello, et al., Single Event Effects characterization of a commercial 28 nm CMOS technology, TWEPP 2023

Weibull fit:

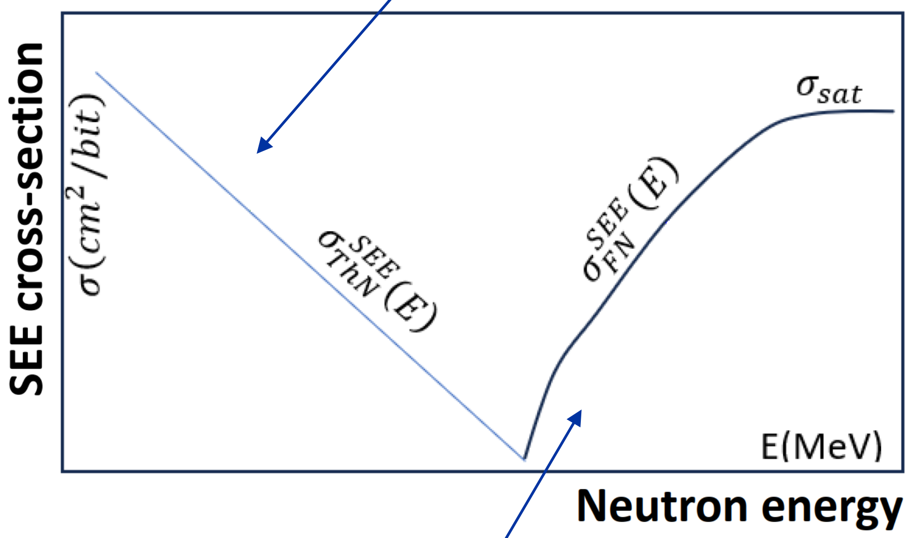
$$\sigma = \boldsymbol{\sigma_\infty}\left(1 - e^{-\left[\frac{LET\ -\ \boldsymbol{LET_0}}{\boldsymbol{W_\sigma}}\right]^{\boldsymbol{s}}}\right)$$

$$n_{th} + {}^{10}\mathrm{B} \rightarrow {}^{4}\mathrm{He}\ (1.47\ \mathrm{MeV}) + {}^{7}\mathrm{Li}\ (0.84\ \mathrm{MeV}) + \gamma\ (0.48\ \mathrm{MeV})$$



thermal neutrons cross section

$\sigma_{ThN}^{SEE}(E) \sim 1/\sqrt{E}$



fast neutrons cross section
weibull fit

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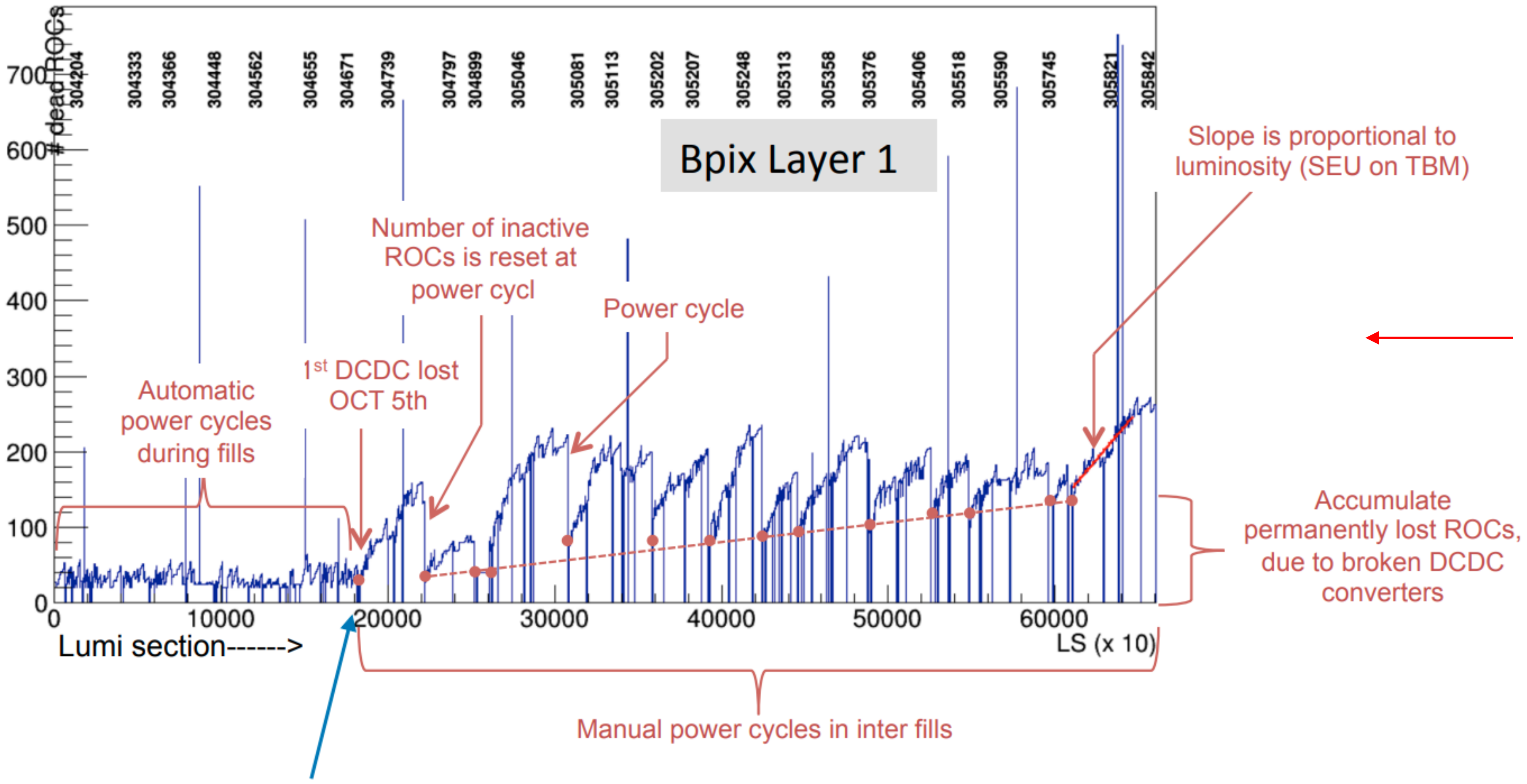
STOCHASTIC	SINGLE EVENT	----

the impact of a single interaction may be almost negligible, but the damage accumulates over time leading to measurable effects

➢ the higher the radiation level, the greater the effects!

failure of DCDC converters in the CMS pixel system during the 2017 run!



caused by TID-induced increase in leakage current of MOS transistors!

Increase in luminosity, change in beam structure

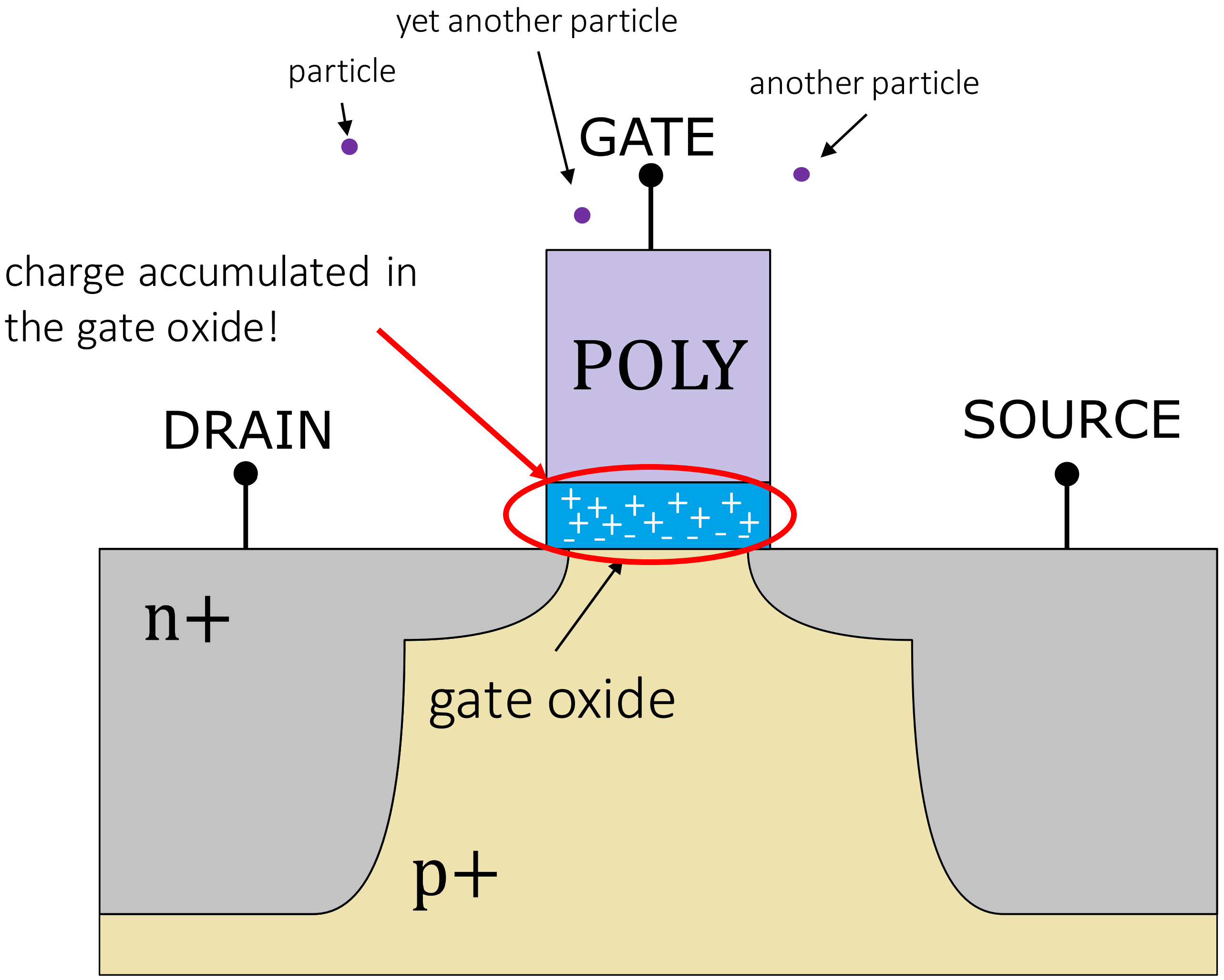
https://indico.desy.de/event/21211/contributions/42055/attachments/26775/33802/KatjaKlein_12thDetectorWorkshop_14032019.pdf
https://espace.cern.ch/project-DCDC-new/Shared%20Documents/SummaryMeasurements18.pdf
https://espace.cern.ch/project-DCDC-new/Shared%20Documents/Report_IRRAD_tests.pdf
https://indico.cern.ch/event/788031/attachments/1794169/2923948/ESE_seminar_Feb19_talk.pdf

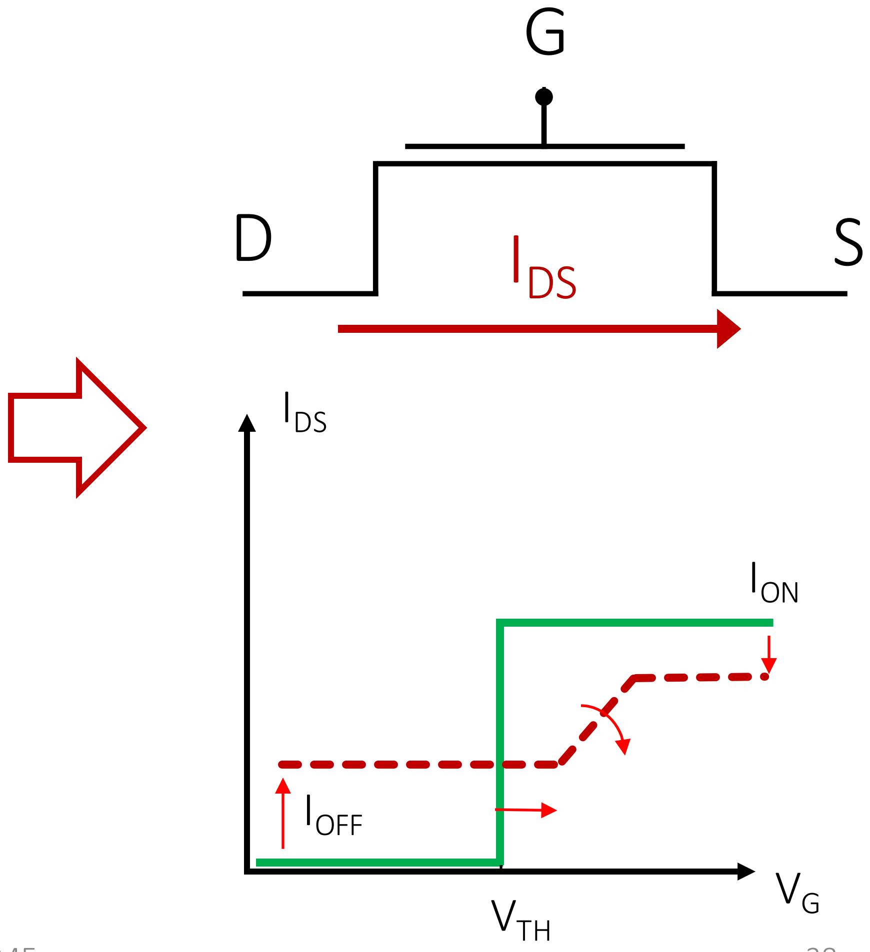
TID effects

≈

accumulation of charge in the oxides of an electronic device

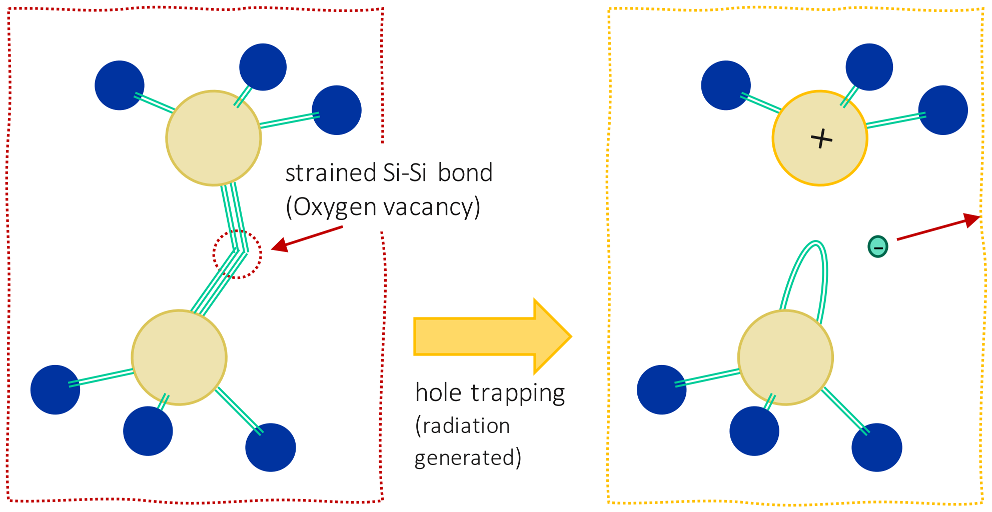
example: charge build-up in the gate oxide of a MOS transistor

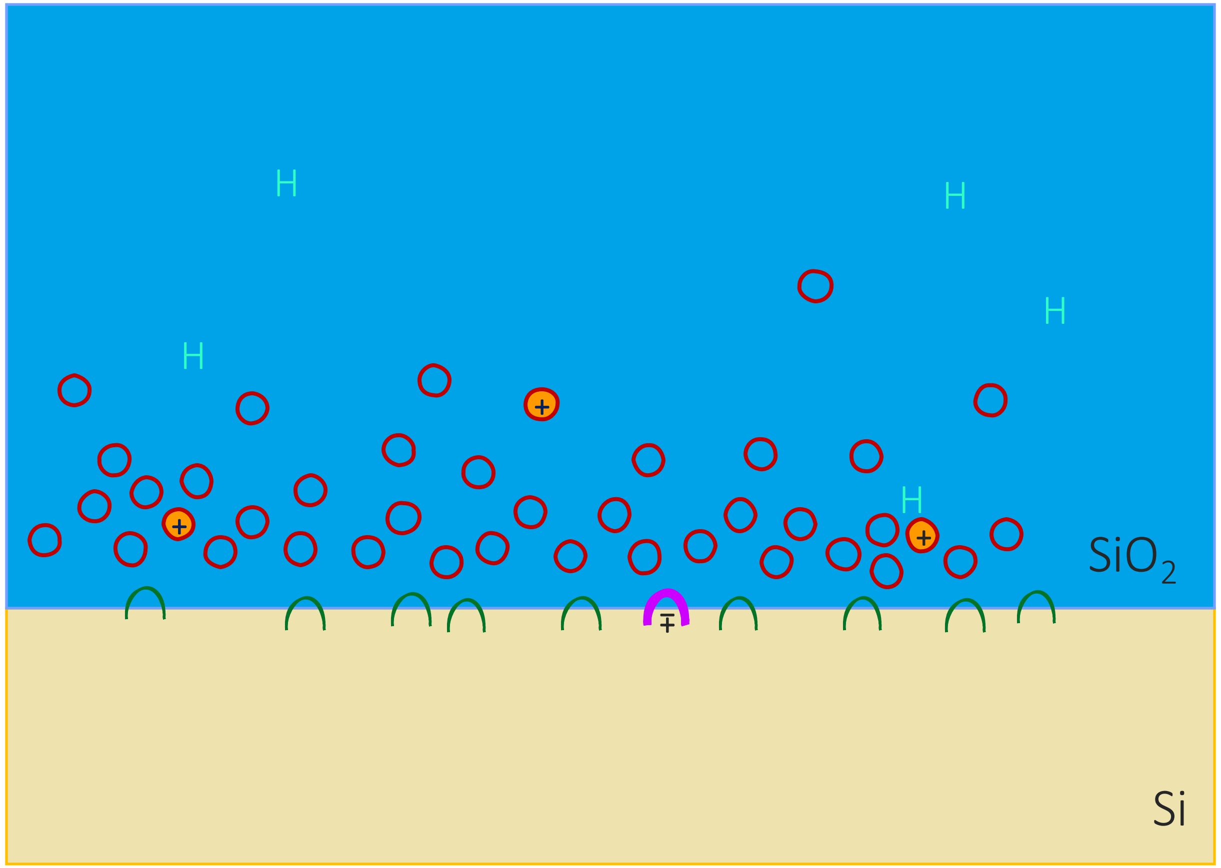




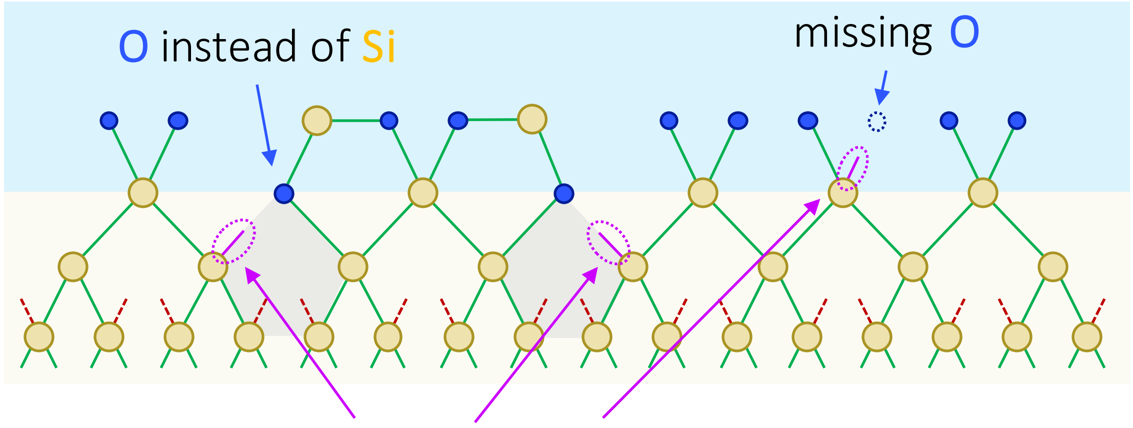
defects in the SiO_2 and/or in
SiO_2/Si interface can trap charge

charge trapped in oxide





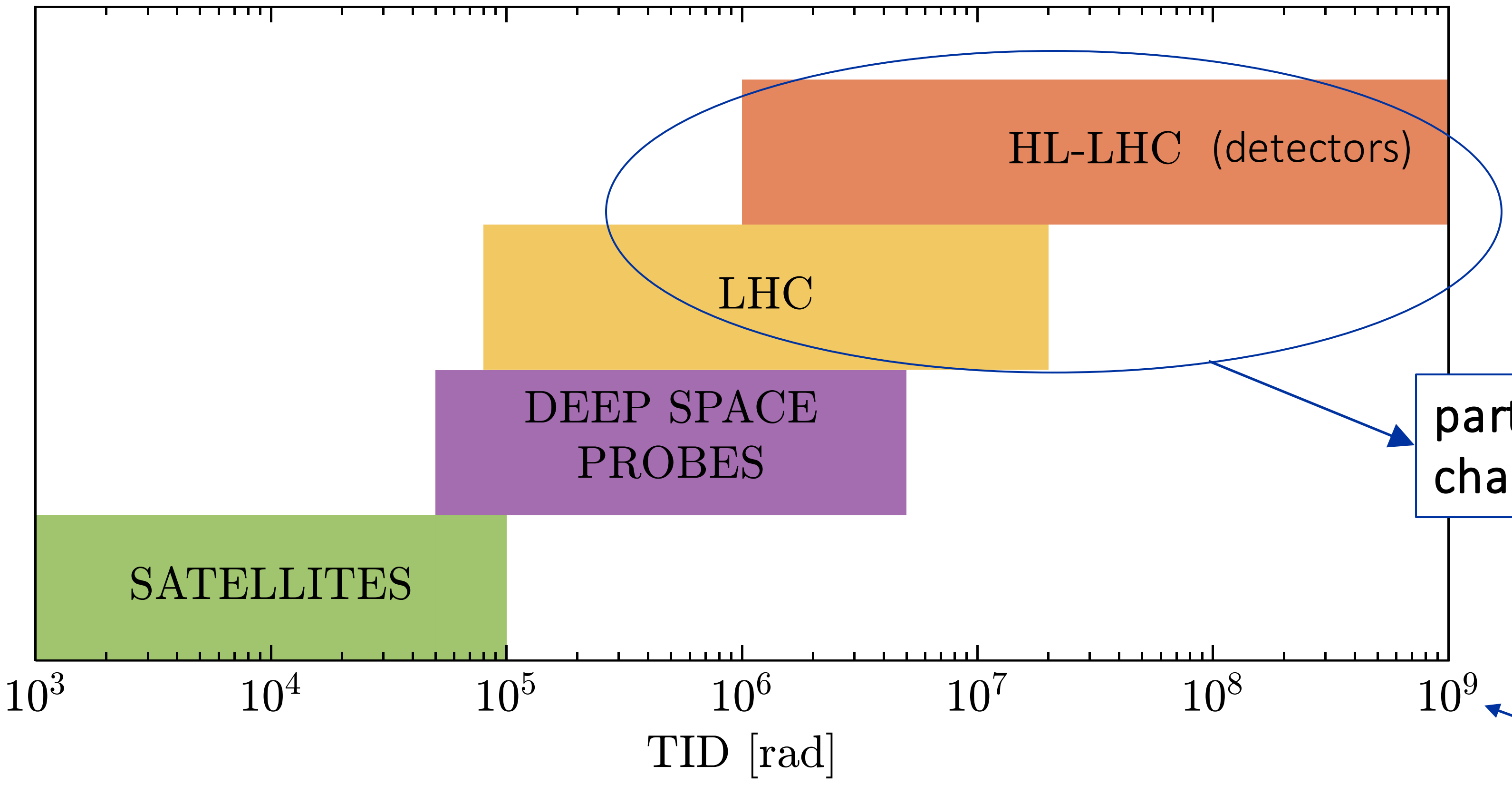
charge trapped at the interface



Unit of measure:

- **gray** (1 Gy = 1 J/Kg; standard unit)
- **rad** (radiation absorbed dose; 1 erg/g)

100 rad = 1 Gy = 1 J/Kg

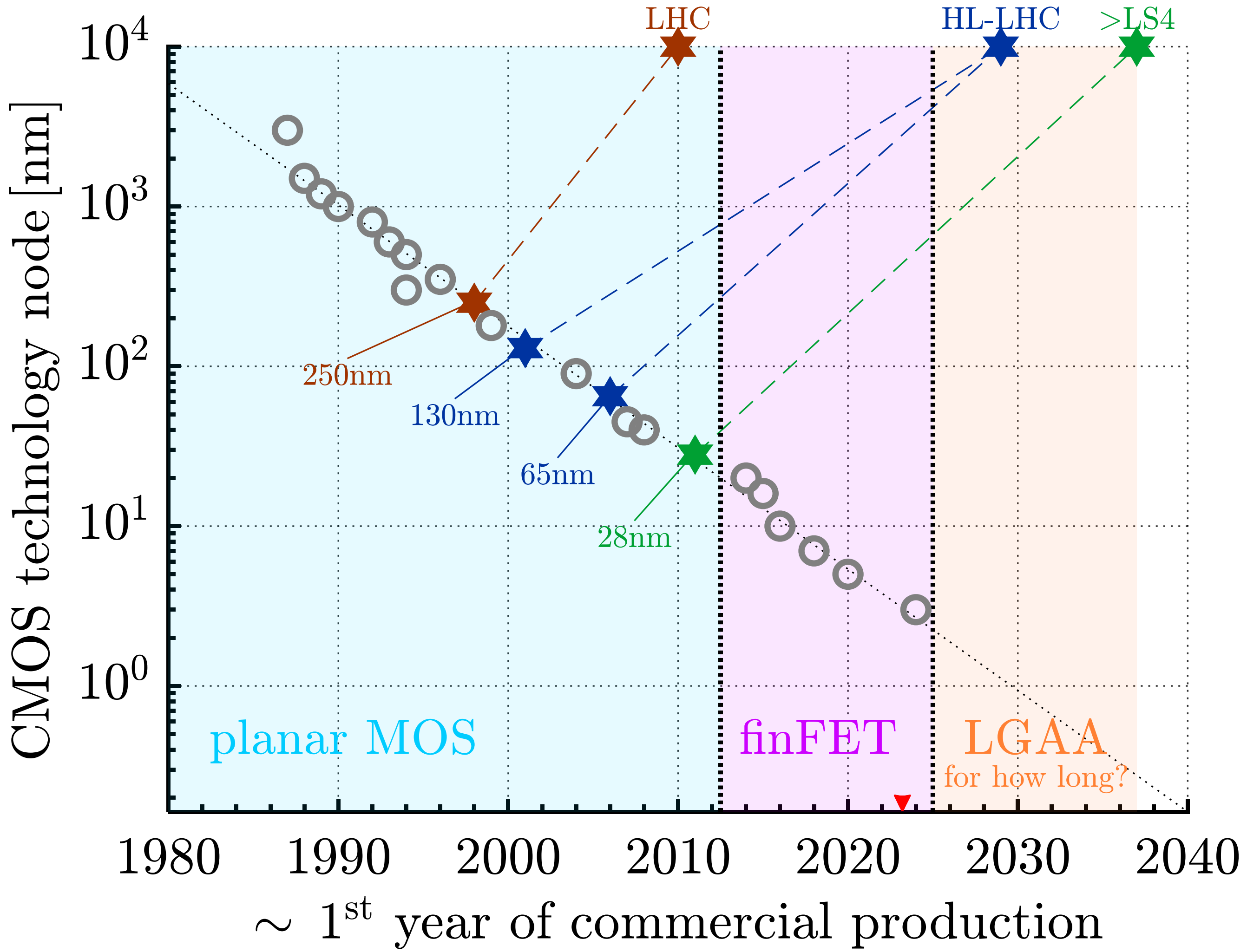


particle accelerators are a very challenging environment!

1 Grad !
(in 10 years)

CERN & CMOS

(detectors)

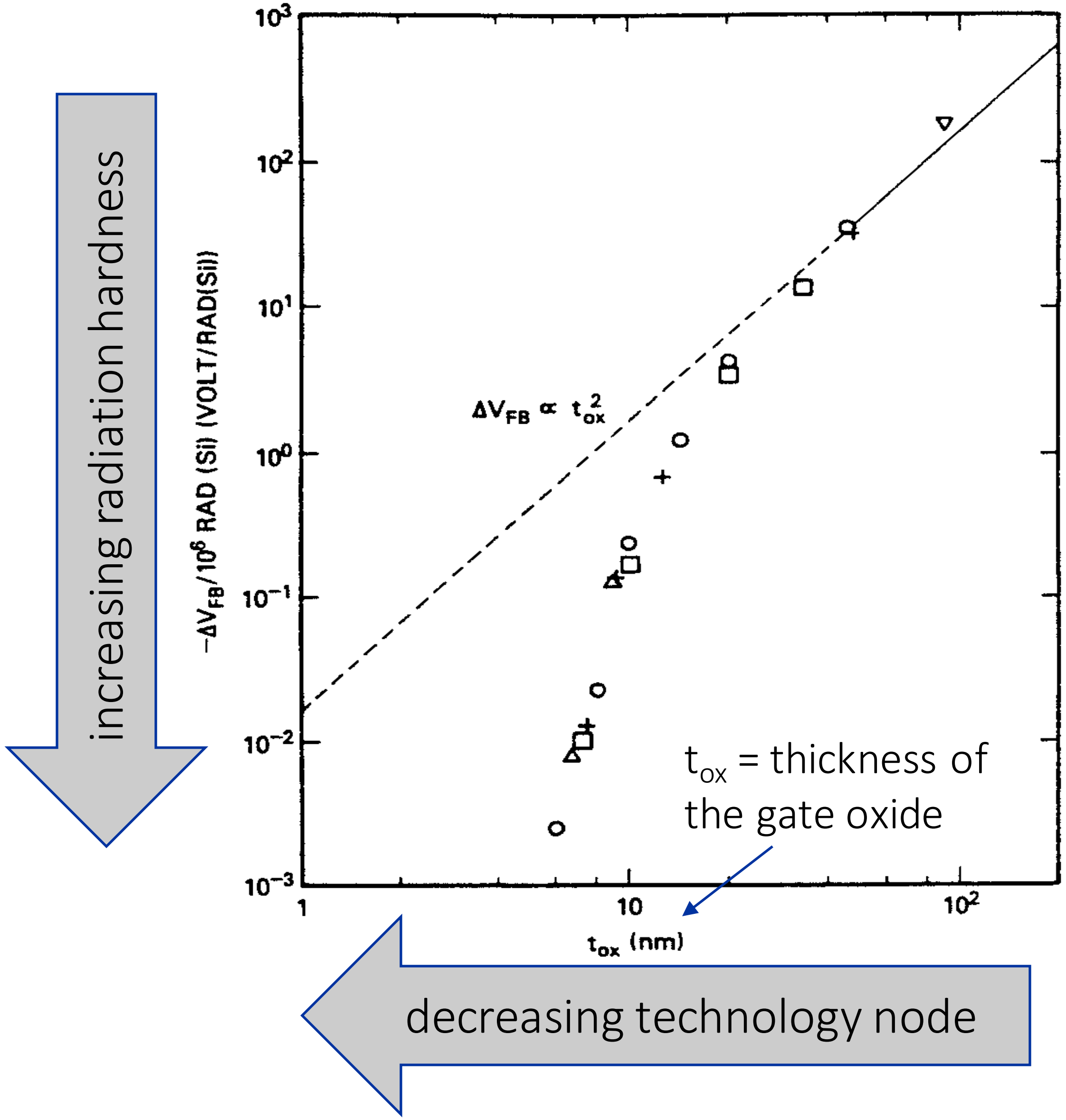


technology scaling
(i.e., smaller transistors)

- + speed
- + density
- - power consumption
- TID hardness (?)

data from:
https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_3nm
https://irds.ieee.org/editions/2022/more-moore

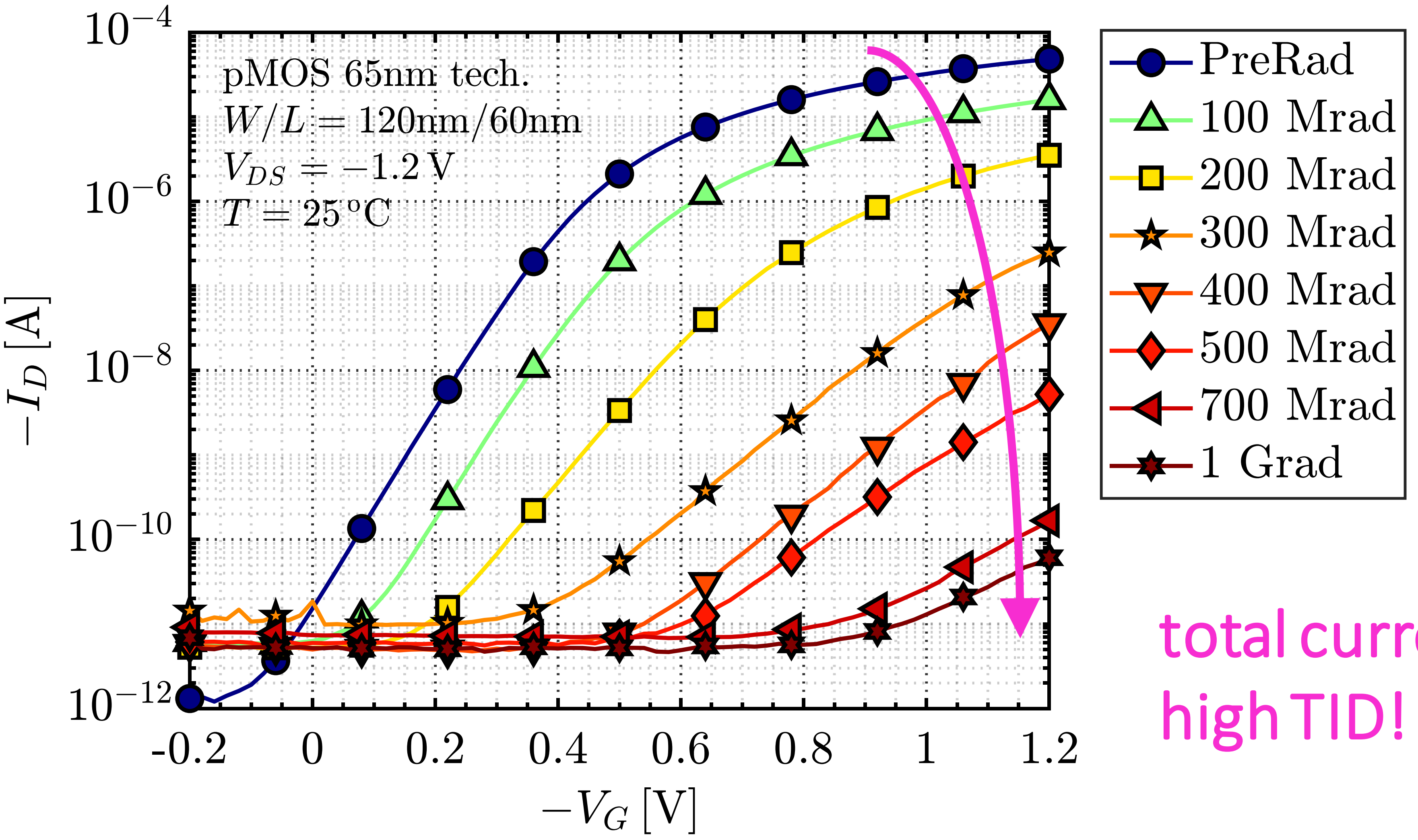
Saks, N. S., et al. IEEE Trans. on Nucl. Sci. 31.6 (1984): 1249-1255.



thin oxides are more rad-hard!!

t_{ox} in 65nm node ≈ 2 nm

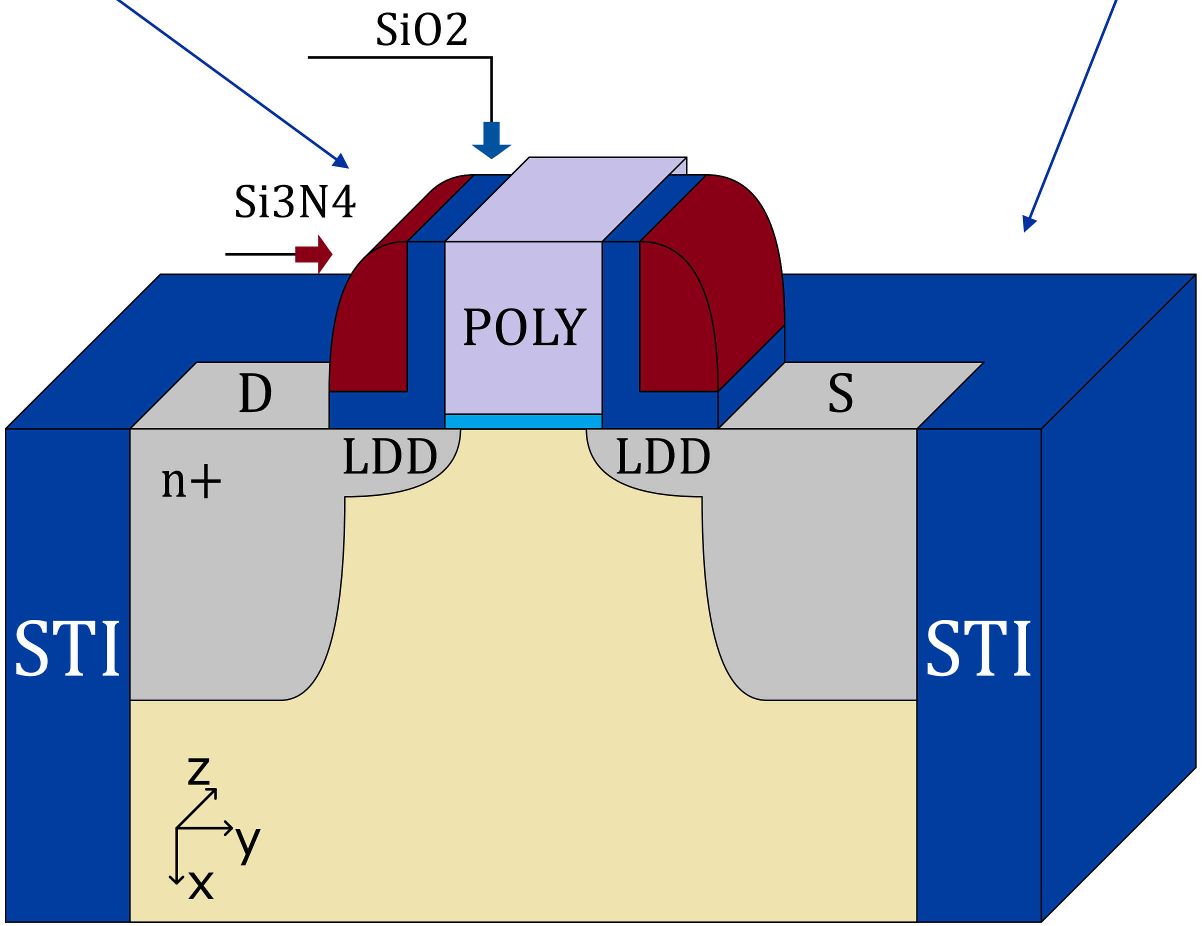
MOSFETs in 65nm CMOS technology should be extremely rad hard!



total current collapse at high TID!

Spacers: needed to create the Lightly Doped Source/Drain (LDD) extensions

Shallow Trench Isolation (STI): useful to isolate adjacent devices



TID effects in modern CMOS technologies are dominated by charge trapped in auxiliary thick oxides like STI and spacers!

STI-related effects

1. radiation-induced drain-to-source **leakage** current
2. radiation-induced **narrow channel** effect (RINCE)
3. halo-enhanced robustness in **short** channels

spacers-related effects

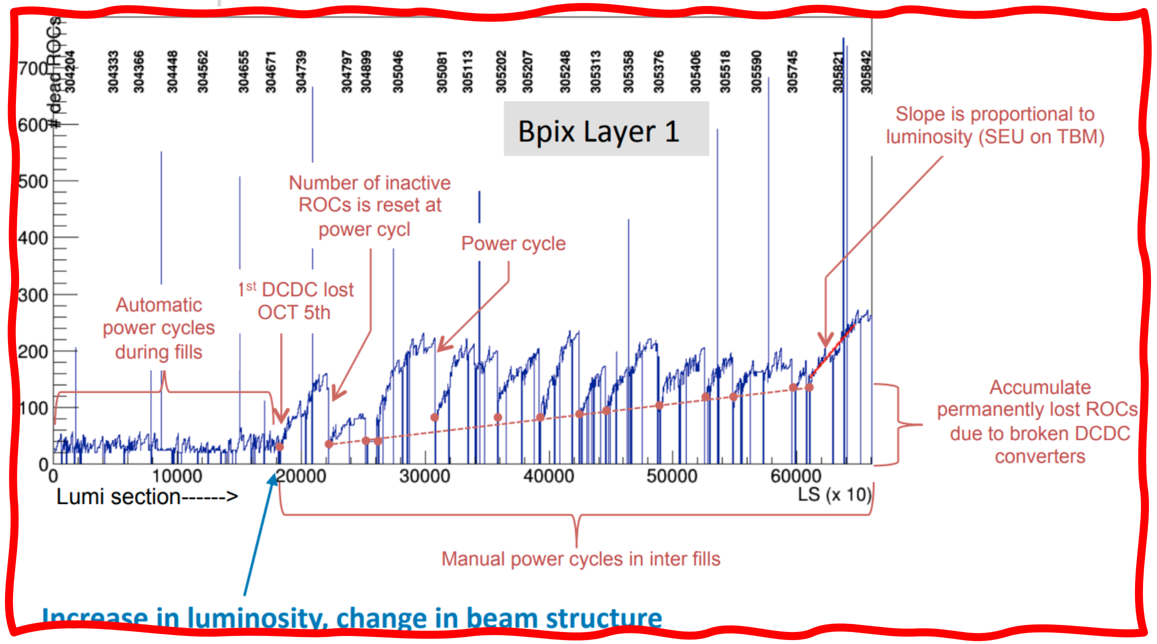
1. radiation-induced **short channel** effect (RISCE)

1. T. R. Oldham, et. al., "Post-Irradiation Effects in Field-Oxide Isolation Structures," in *IEEE Transactions on Nuclear Science*, vol. 34, no. 6, pp. 1184-1189, Dec. 1987.
2. M. R. Shaneyfelt et. al, "Challenges in hardening technologies using shallow-trench isolation," in *IEEE Transactions on Nuclear Science*, vol. 45, no. 6, pp. 2584-2592, Dec. 1998.
3. A. H. Johnston, et. al, "Total Dose Effects in CMOS Trench Isolation Regions," in *IEEE Transactions on Nuclear Science*, vol. 56, no. 4, pp. 1941-1949, Aug. 2009.
4. Nadia Rezzak, et. al, "The sensitivity of radiation-induced leakage to STI topology and sidewall doping", *Microelectronics Reliability*, Volume 51, Issue 5, 2011, Pages 889-894.
5. C. -M. Zhang et al., "Characterization and Modeling of Gigarad-TID-Induced Drain Leakage Current of 28-nm Bulk MOSFETs," in *IEEE Transactions on Nuclear Science*, vol. 66, no. 1, pp. 38-47, Jan. 2019
6. Faccio, Federico, and Giovanni Cervelli. "Radiation-induced edge effects in deep submicron CMOS transistors." IEEE Transactions on Nuclear Science 52.6 (2005): 2413-2420.
7. Gaillardin, M., et al. "Enhanced Radiation-Induced Narrow Channel Effects in Commercial ${\hbox {0.18}}~\mu $ m Bulk Technology." IEEE Transactions on Nuclear Science 58.6 (2011): 2807-2815.
8. Faccio, F., et al. "Radiation-induced short channel (RISCE) and narrow channel (RINCE) effects in 65 and 130 nm MOSFETs." IEEE Transactions on Nuclear Science 62.6 (2015): 2933-2940.
9. Bonaldo, S., et al. "Influence of halo implantations on the total ionizing dose response of 28-nm pMOSFETs irradiated to ultrahigh doses." IEEE Transactions on Nuclear Science 66.1 (2018): 82-90.
10. Bonaldo, S., et al. "Ionizing-radiation response and low-frequency noise of 28-nm MOSFETs at ultrahigh doses." IEEE Transactions on Nuclear Science 67.7 (2020): 1302-1311.
11. F. Faccio, et. L,, "Radiation-Induced Short Channel (RISCE) and Narrow Channel (RINCE) Effects in 65 and 130 nm MOSFETs," in *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2933-2940, Dec. 2015
12. F. Faccio *et al.*, "Influence of LDD Spacers and H+ Transport on the Total-Ionizing-Dose Response of 65-nm MOSFETs Irradiated to Ultrahigh Doses," in *IEEE Transactions on Nuclear Science*, vol. 65, no. 1, pp. 164-174, Jan. 2018
13. S. Bonaldo et al., "Charge Buildup and Spatial Distribution of Interface Traps in 65-nm pMOSFETs Irradiated to Ultrahigh Doses," in IEEE Transactions on Nuclear Science, vol. 66, no. 7, pp. 1574-1583, July 2019

STI-related effects

spacers-related effects

1. radiation-induced drain-to-source **leakage** current
2. radiation-induced **narrow channel** effect (RINCE)
3. halo-enhanced robustness in **short** channels



1. T. R. Oldham, et. al., "Post-Irradiation Effects in Field-Oxide Isolation Structures," in *IEEE Transactions on Nuclear Science*, vol. 34, no. 6, pp. 1184-1189, Dec. 1987.
2. M. R. Shaneyfelt et. al, "Challenges in hardening technologies using shallow-trench isolation," in *IEEE Transactions on Nuclear Science*, vol. 45, no. 6, pp. 2584-2592, Dec. 1998.
3. A. H. Johnston, et. al, "Total Dose Effects in CMOS Trench Isolation Regions," in *IEEE Transactions on Nuclear Science*, vol. 56, no. 4, pp. 1941-1949, Aug. 2009.
4. Nadia Rezzak, et. al, “The sensitivity of radiation-induced leakage to STI topology and sidewall doping”, *Microelectronics Reliability*, Volume 51, Issue 5, 2011, Pages 889-894.
5. C. -M. Zhang et al., "Characterization and Modeling of Gigarad-TID-Induced Drain Leakage Current of 28-nm Bulk MOSFETs," in *IEEE Transactions on Nuclear Science*, vol. 66, no. 1, pp. 38-47, Jan. 2019
6. Faccio, Federico, and Giovanni Cervelli. "Radiation-induced edge effects in deep submicron CMOS transistors." IEEE Transactions on Nuclear Science 52.6 (2005): 2413-2420.
7. Gaillardin, M., et al. "Enhanced Radiation-Induced Narrow Channel Effects in Commercial ${\hbox {0.18}}~\mu $ m Bulk Technology." IEEE Transactions on Nuclear Science 58.6 (2011): 2807-2815.
8. Faccio, F., et al. "Radiation-induced short channel (RISCE) and narrow channel (RINCE) effects in 65 and 130 nm MOSFETs." IEEE Transactions on Nuclear Science 62.6 (2015): 2933-2940.
9. Bonaldo, S., et al. "Influence of halo implantations on the total ionizing dose response of 28-nm pMOSFETs irradiated to ultrahigh doses." IEEE Transactions on Nuclear Science 66.1 (2018): 82-90.
10. Bonaldo, S., et al. "Ionizing-radiation response and low-frequency noise of 28-nm MOSFETs at ultrahigh doses." IEEE Transactions on Nuclear Science 67.7 (2020): 1302-1311.
11. F. Faccio, et. L,, "Radiation-Induced Short Channel (RISCE) and Narrow Channel (RINCE) Effects in 65 and 130 nm MOSFETs," in *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2933-2940, Dec. 2015
12. F. Faccio *et al.*, "Influence of LDD Spacers and H+ Transport on the Total-Ionizing-Dose Response of 65-nm MOSFETs Irradiated to Ultrahigh Doses," in *IEEE Transactions on Nuclear Science*, vol. 65, no. 1, pp. 164-174, Jan. 2018
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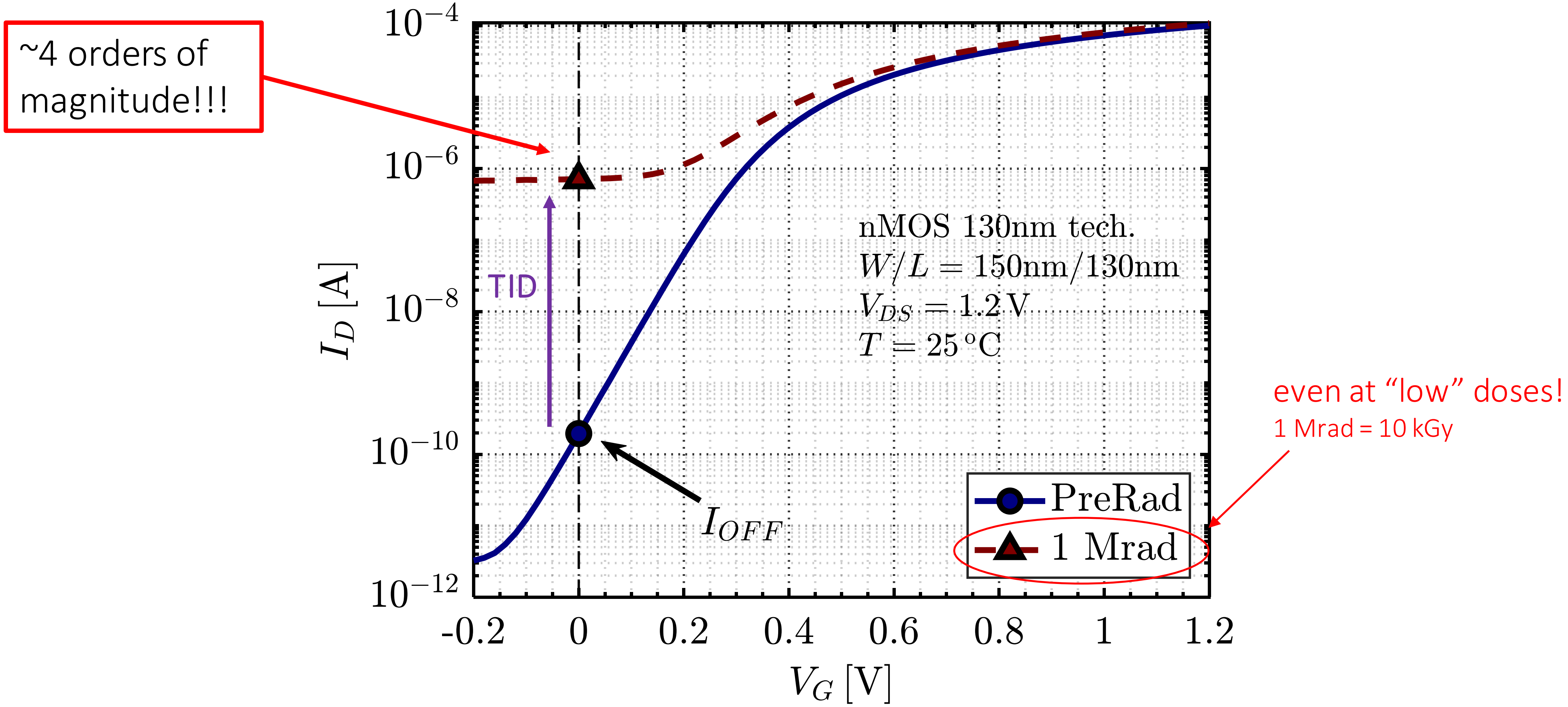
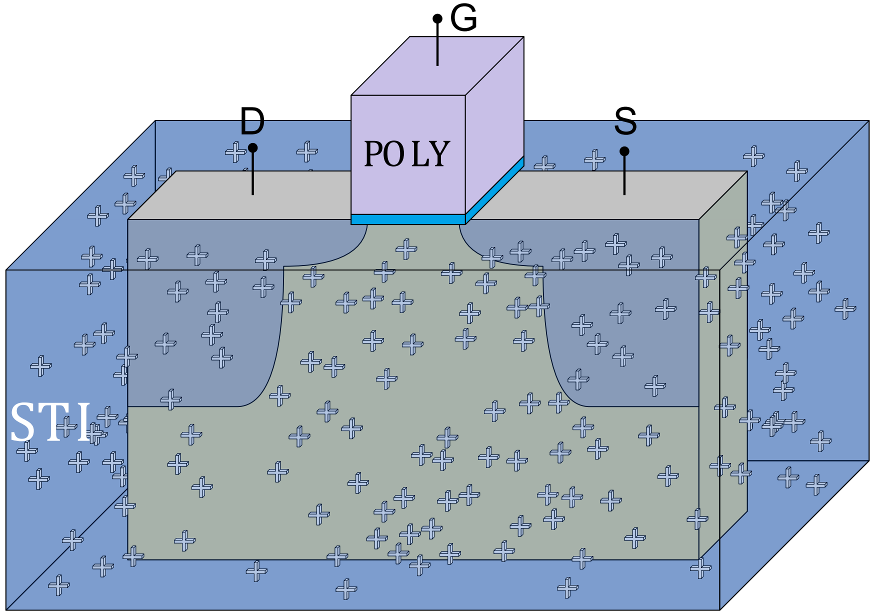
leakage current: $I_{OFF} = I_{DS}(V_{GS} = 0\ V, V_{DS} = V_{DD})$

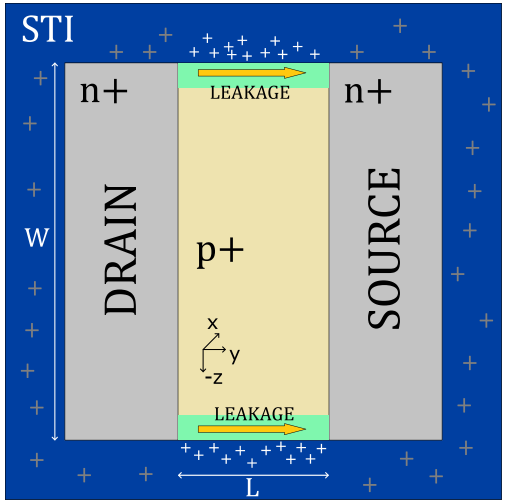
(e.g., static power consumption of a CMOS inverter: $P_S = V_{DD} \times I_{OFF}$)

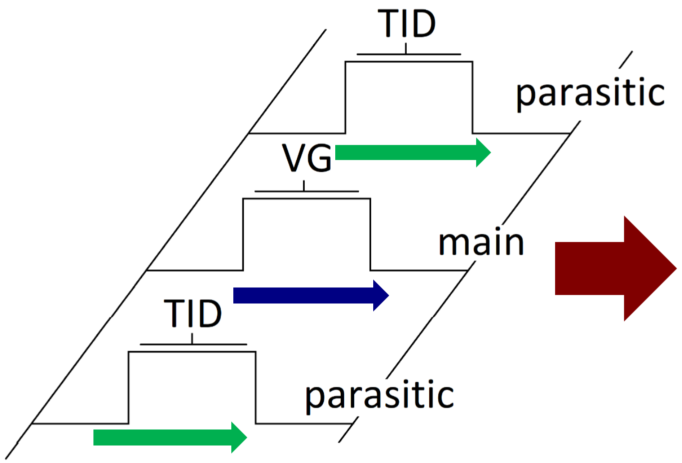


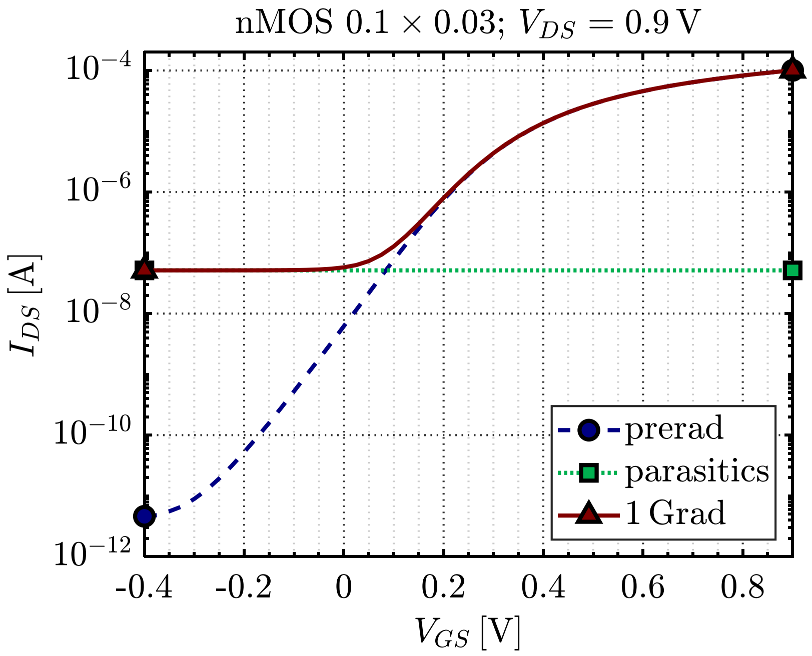


radiation-induced charge in the STI

top view
without
gate

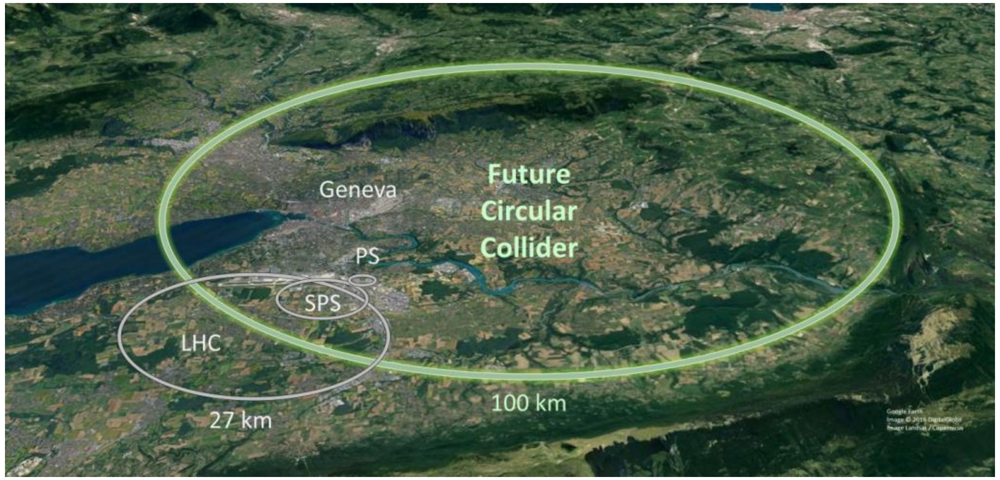




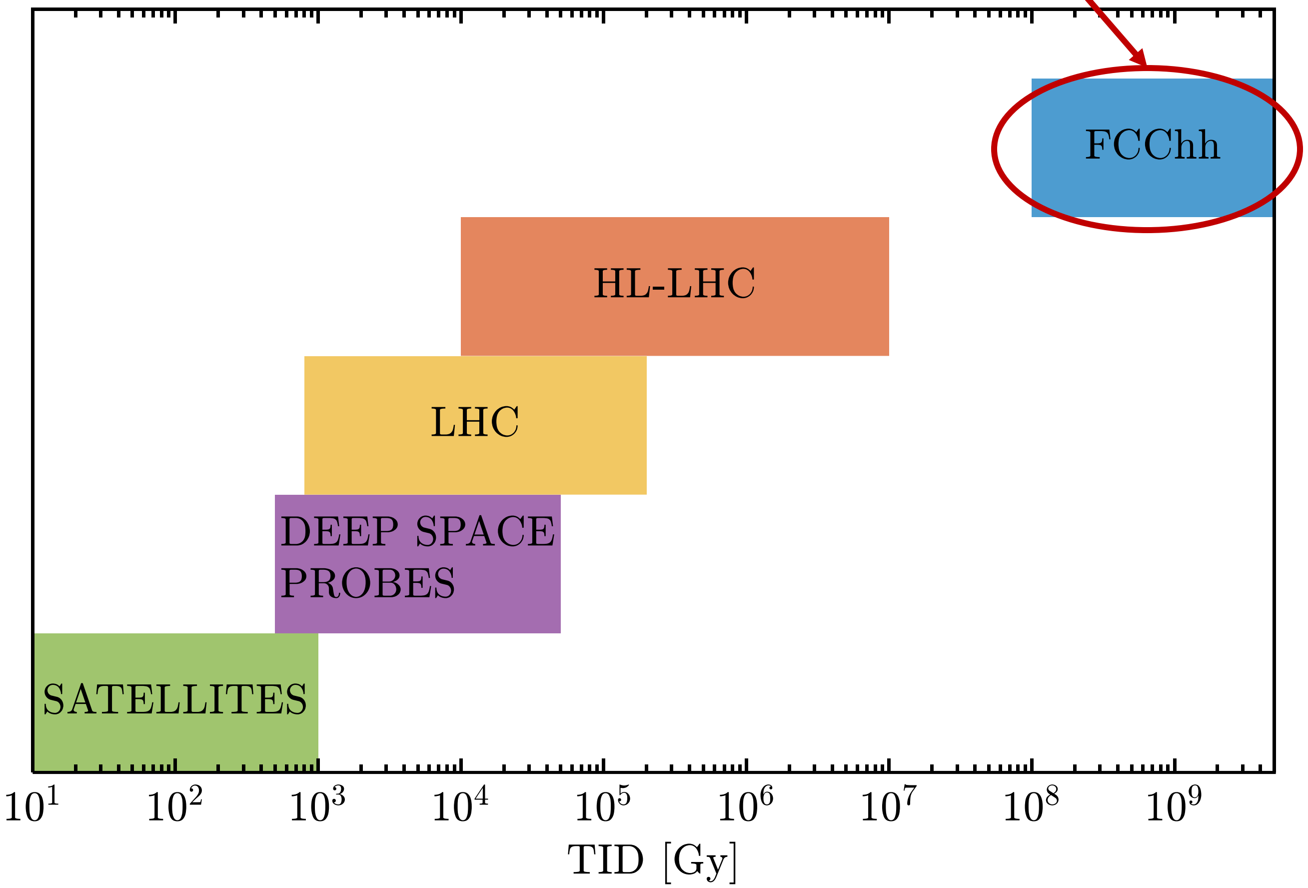


Future Circular Collider (FCChh)

https://home.cern/science/accelerators/future-circular-collider



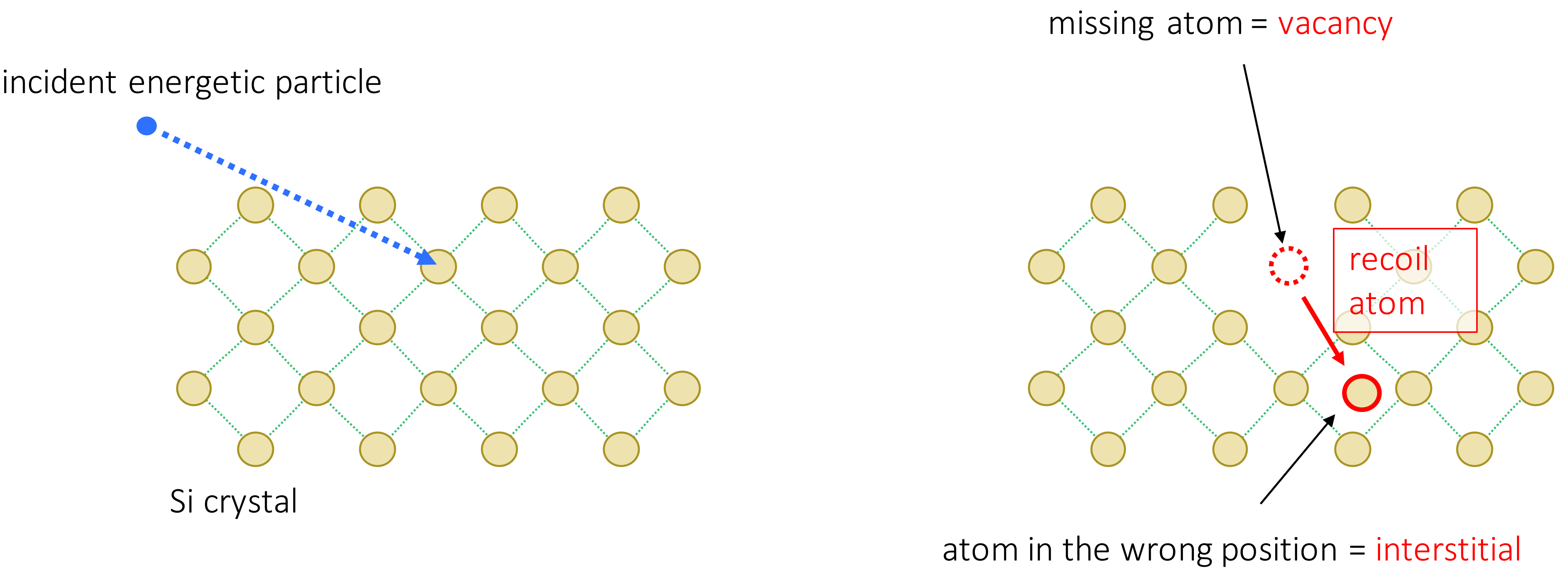
10-500 Grad!!!*



*https://indico.cern.ch/event/656491/contributions/2915679/attachments/1629768/2601671/20180412_INFANTINO_ST_R2E_overview.pdf

RADIATION EFFECTS	IONIZING	NON-IONIZING
CUMULATIVE	TOTAL IONIZING DOSE (TID)	DISPLACEMENT DAMAGE
STOCHASTIC	SINGLE EVENT EFFECTS	-----------------------

physical mechanisms of DD-induced degradation



The disturbance in the crystal lattice periodicity has associated discrete energy levels in the forbidden energy band-gap. These influence generation-recombination processes in the material.

[1] J. R. Srour, C. J. Marshall and P. W. Marshall, "Review of displacement damage effects in silicon devices," in *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 653-670, June 2003, doi: 10.1109/TNS.2003.813197.
[2] Oldham, Timothy R. "Basic mechanisms of TID and DDD response in MOS and bipolar microelectronics." *NSREC Short Course* (2011).
[3] J. R. Srour and J. W. Palko, "Displacement Damage Effects in Irradiated Semiconductor Devices," in *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1740-1766, June 2013, doi: 10.1109/TNS.2013.2261316.

DD is problematic mainly for:

- Bipolar transistors
  - Barnaby, Hugh J., et al. "Displacement damage in bipolar junction transistors: Beyond Messenger-Spratt." IEEE Transactions on Nuclear Science 64.1 (2016): 149-155
  - Rax, B. G., A. H. Johnston, and T. Miyahira. "Displacement damage in bipolar linear integrated circuits." IEEE Transactions on Nuclear Science 46.6 (1999): 1660-1665.

- Particle detectors/image sensors/diodes
  - Moll, Michael. "Displacement damage in silicon detectors for high energy physics." IEEE Transactions on Nuclear Science 65.8 (2018): 1561-1582.

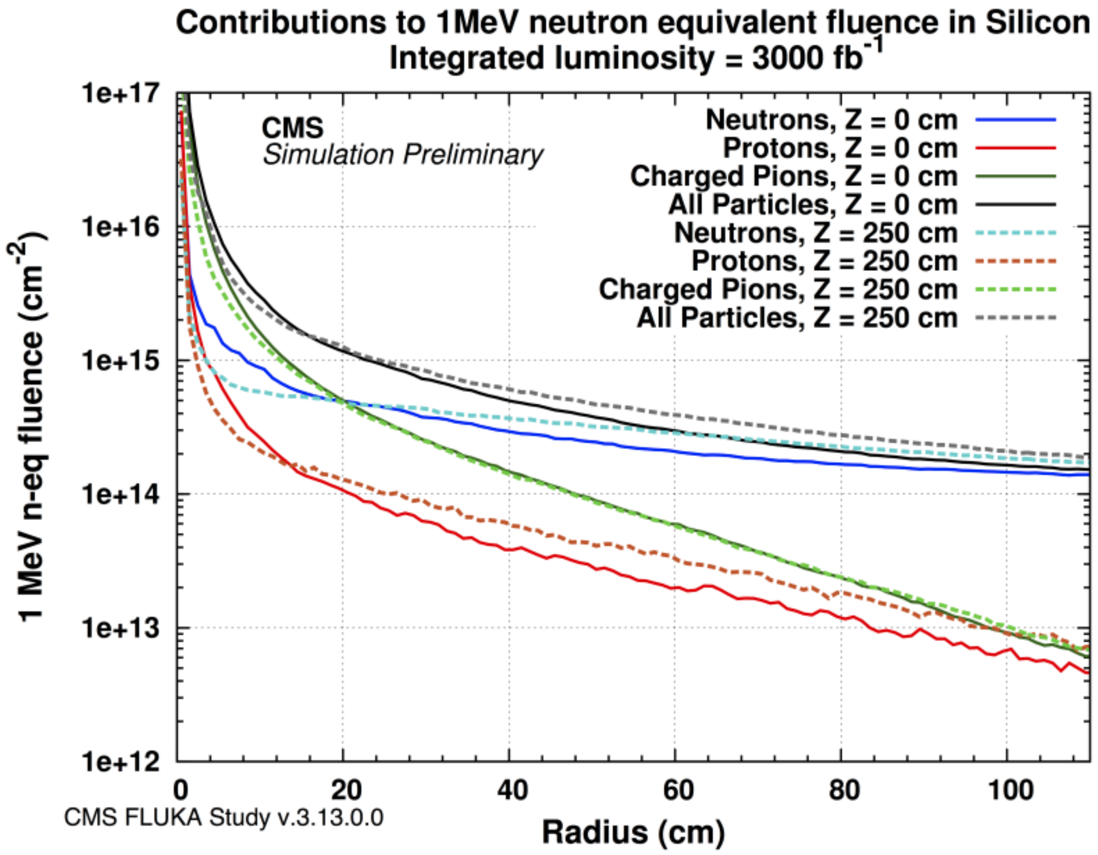
➢ MOS transistors are typically immune to DD
  - !! Except for power MOSFETs
  - Faccio, Federico, et al. "TID and displacement damage effects in vertical and lateral power MOSFETs for integrated DC-DC converters." 2009 RADECs. IEEE, 2009.

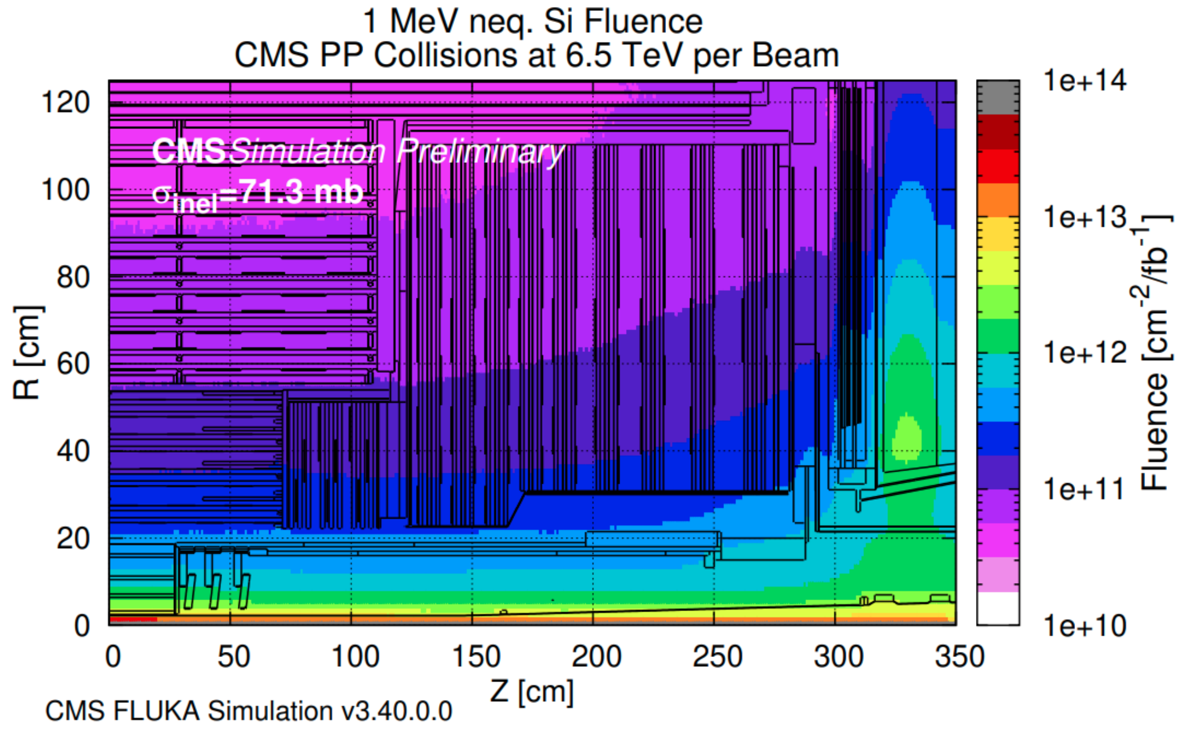
QUESTIONS?

RADIATION EFFECTS	IONIZING	NON-IONIZING
CUMULATIVE	TOTAL IONIZING DOSE (TID)	DISPLACEMENT DAMAGE
STOCHASTIC	SINGLE EVENT EFFECTS	------------------------

EXTRA

https://www.youtube.com/watch?v=bhBf5crp0i8&ab_channel=UncommentatedPannen

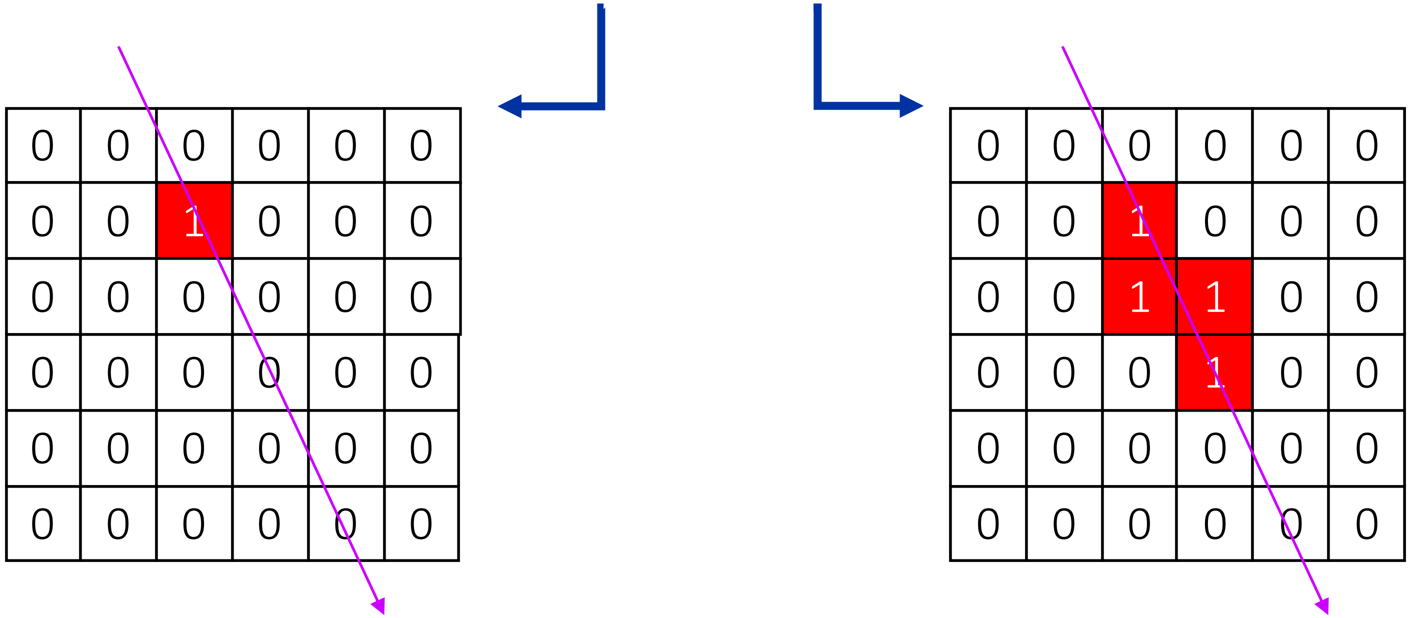




https://cds.cern.ch/record/2773266/files/10.23731_CYRM-2021-001.35.pdf

BIT-UPSET = change in the value of a bit caused by a particle

single- and multi-bit-upsets (SBU, MBU)



Single Event Effects

non-destructive

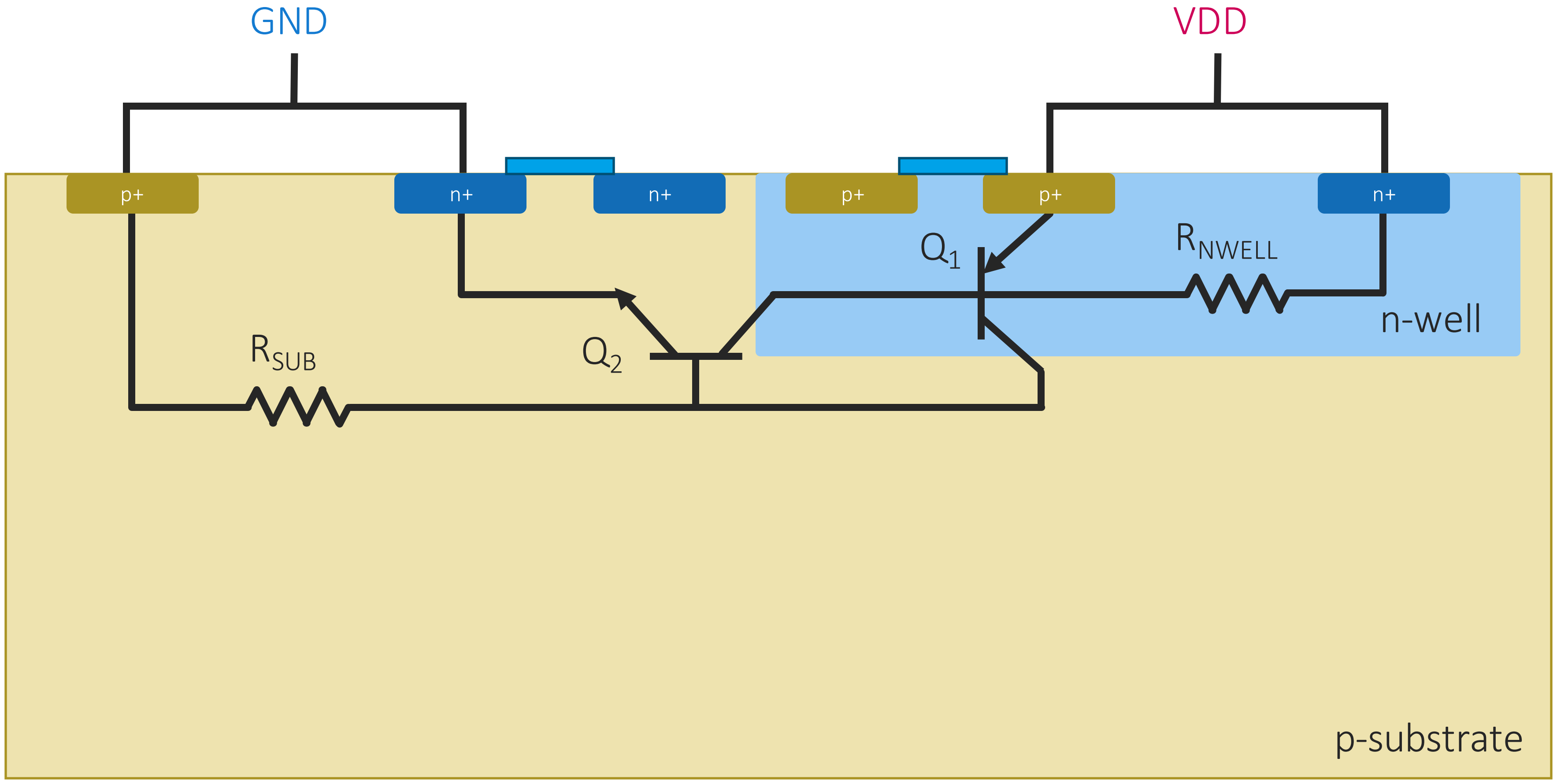
- Single/Multi Event Upset
- Single Event Transient
- etc…

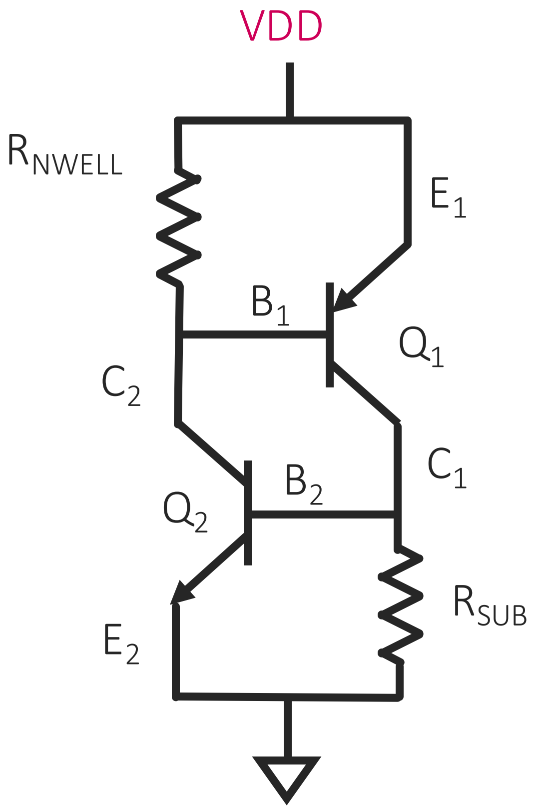
destructive

- Single Event Latch-Up
  (potentially destructive)
- Single Event Burn-out
- Single Event Gate Rupture
- etc…

ON/OFF power cycling
or replacement if destructive

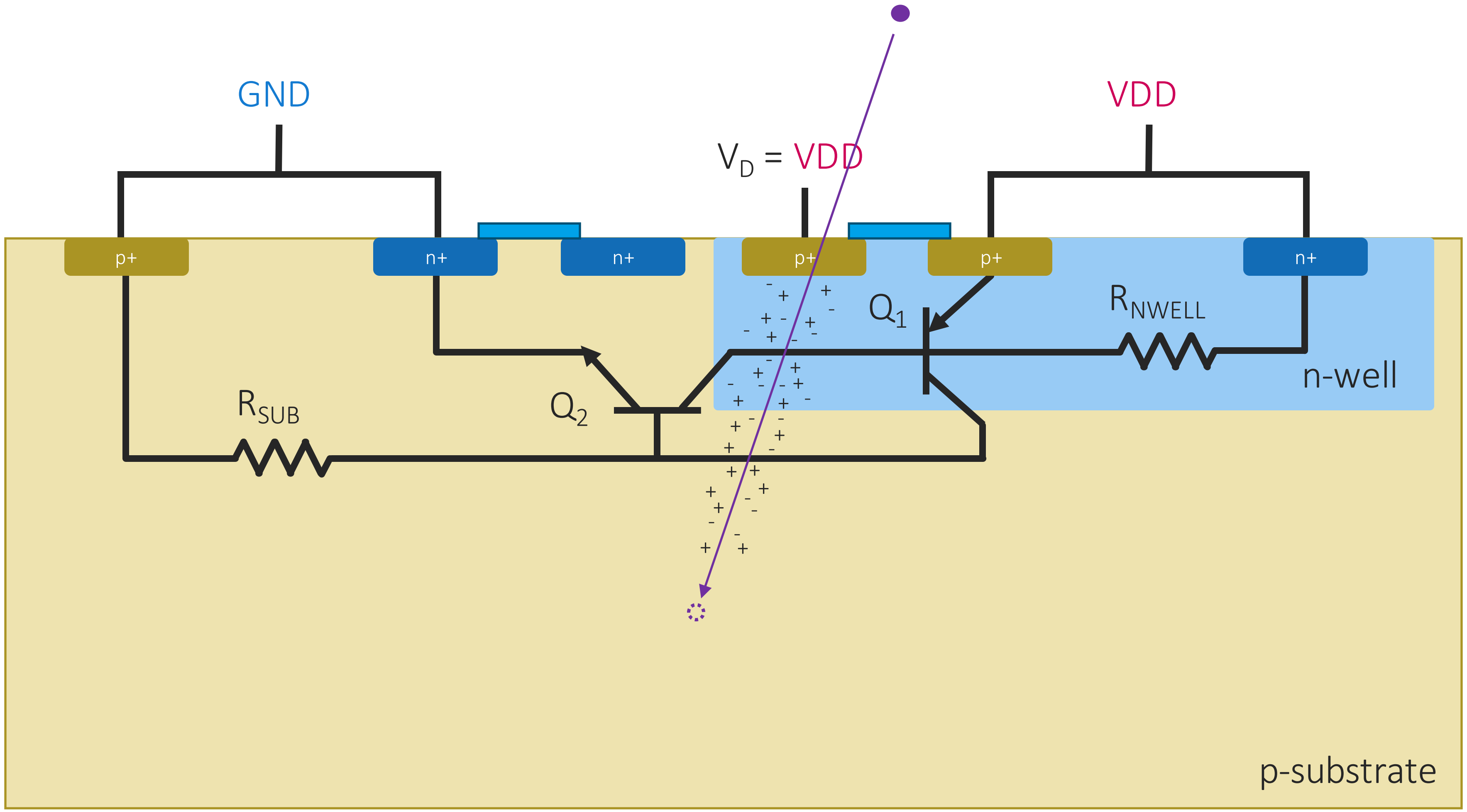
SINGLE EVENT LATCH-UP (SEL)

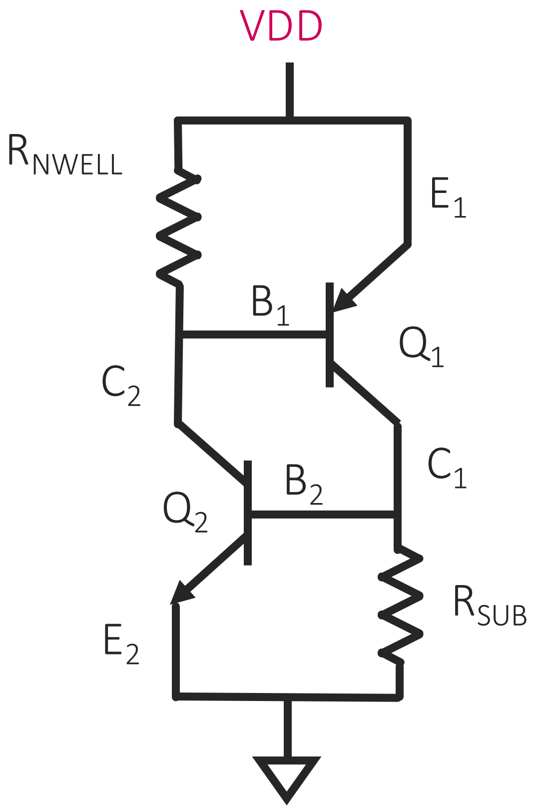




SINGLE EVENT LATCH-UP (SEL)

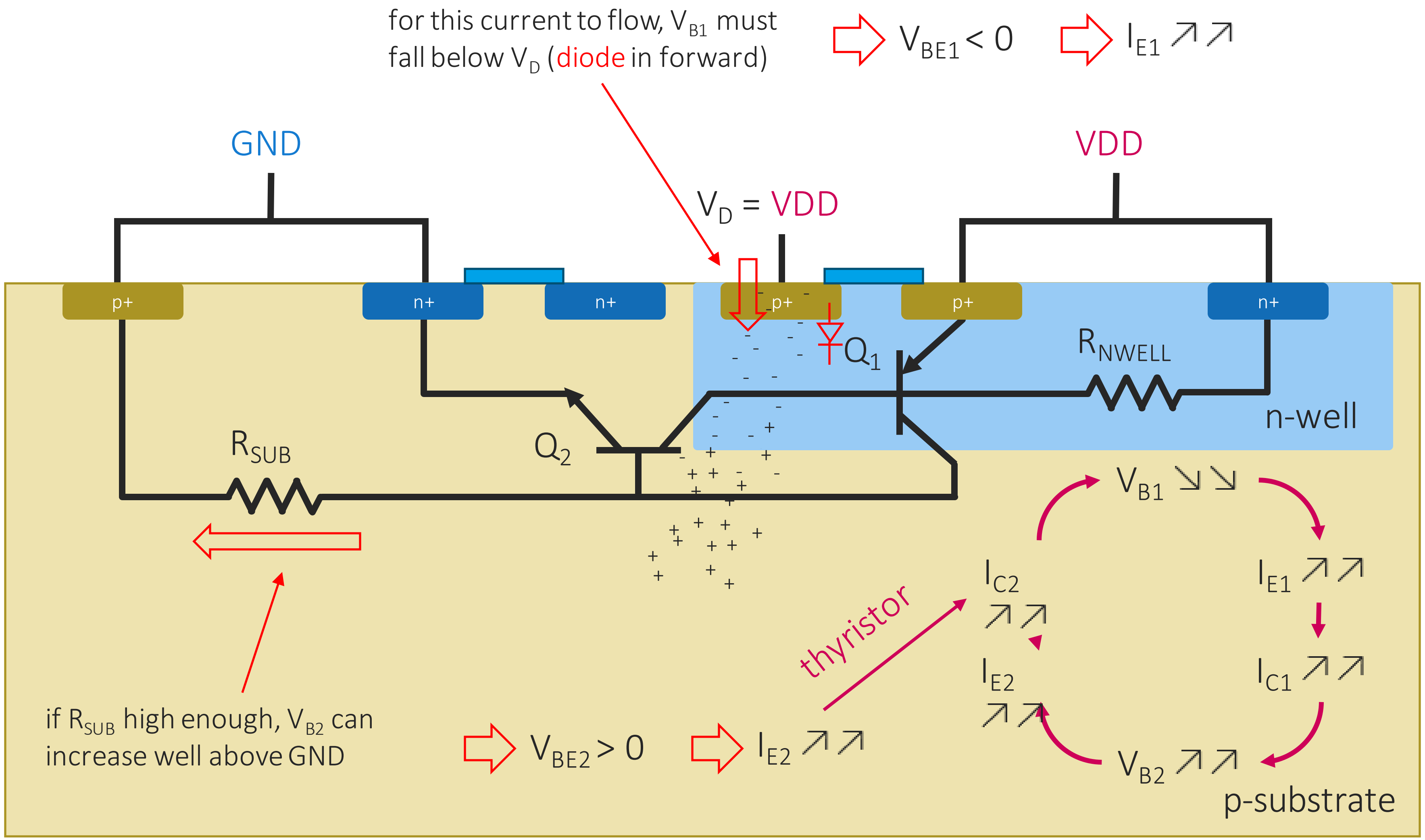
$$I_E = I_S\left(e^{\frac{\pm V_{BE}}{V_{th}}} - 1\right)$$
$$I_C = \alpha_F I_E$$
$$I_B = (1-\alpha_F)I_E$$

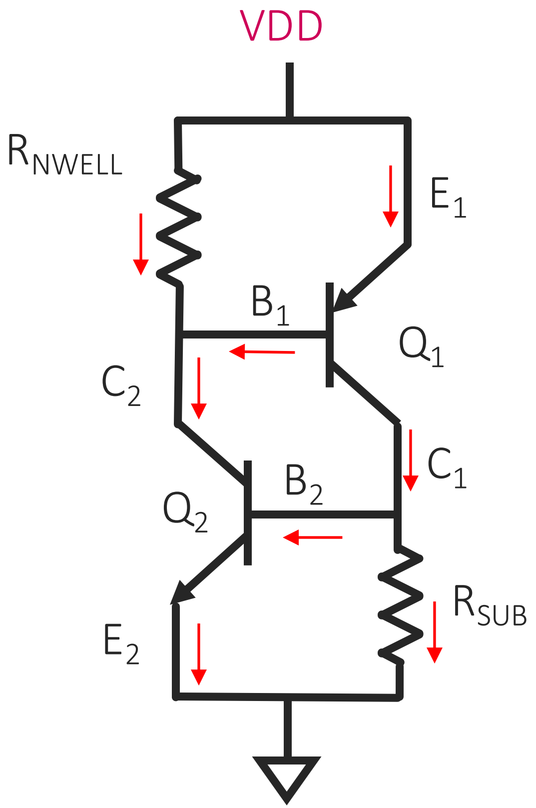


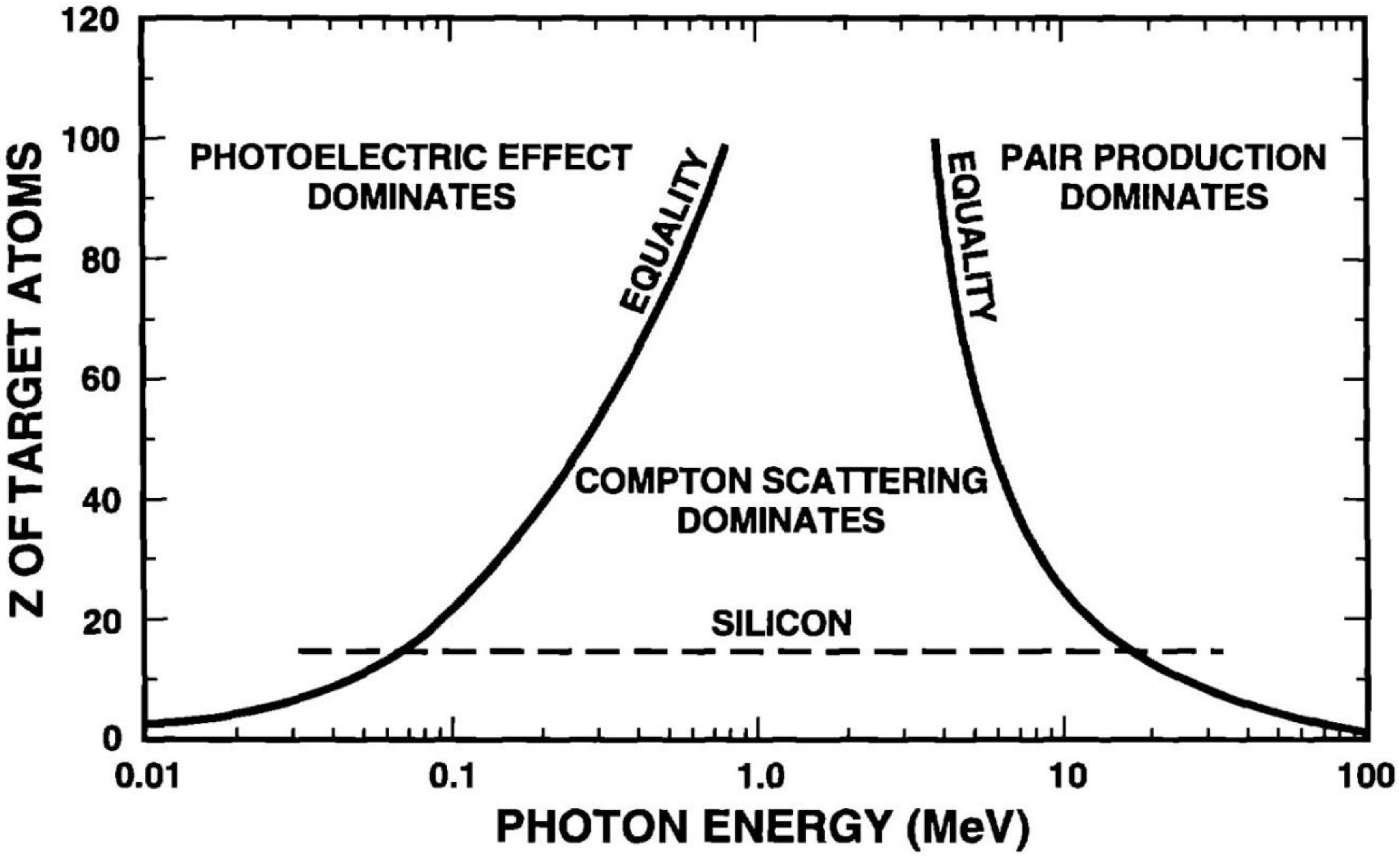


SINGLE EVENT LATCH-UP (SEL)

$$I_E = I_S\left(e^{\frac{\pm V_{BE}}{V_{th}}} - 1\right)$$
$$I_C = \alpha_F I_E$$
$$I_B = (1-\alpha_F) I_E$$



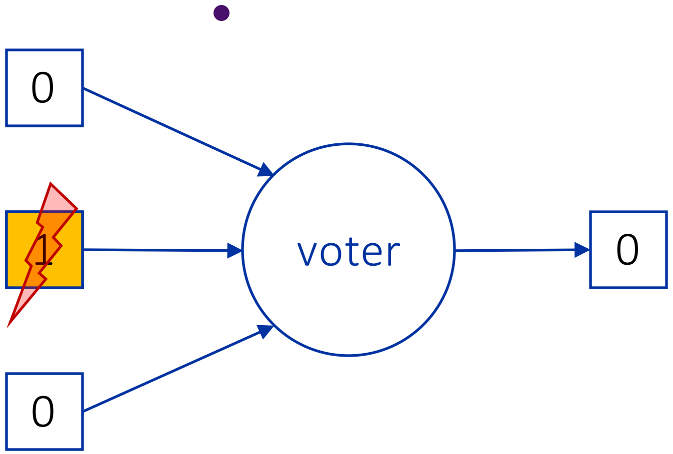




R. D. Evans. *The atomic nucleus*. McGraw-Hill New York, 1955.

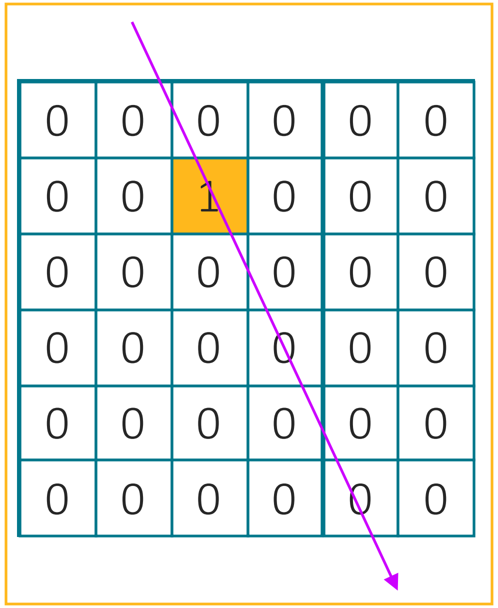
TRIPLICATION

(widely used to prevent SEU)

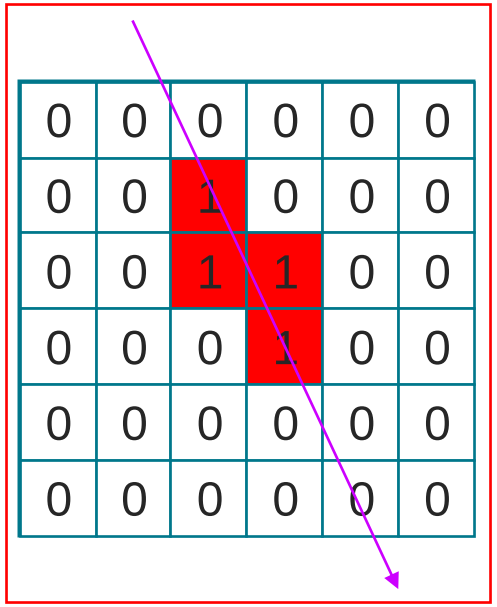


BIT-UPSET = change in the value of a bit caused by a particle

Single-bit-upset (SBU)

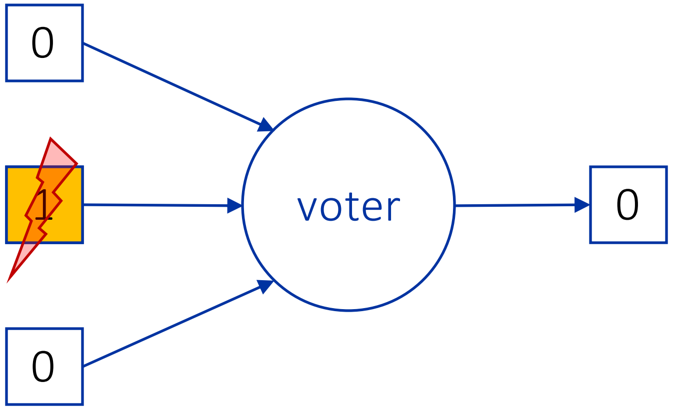


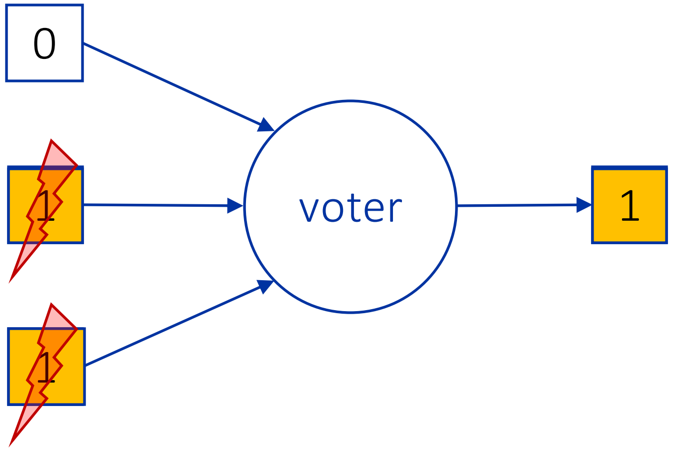
Multi-bit-upset (MBU)

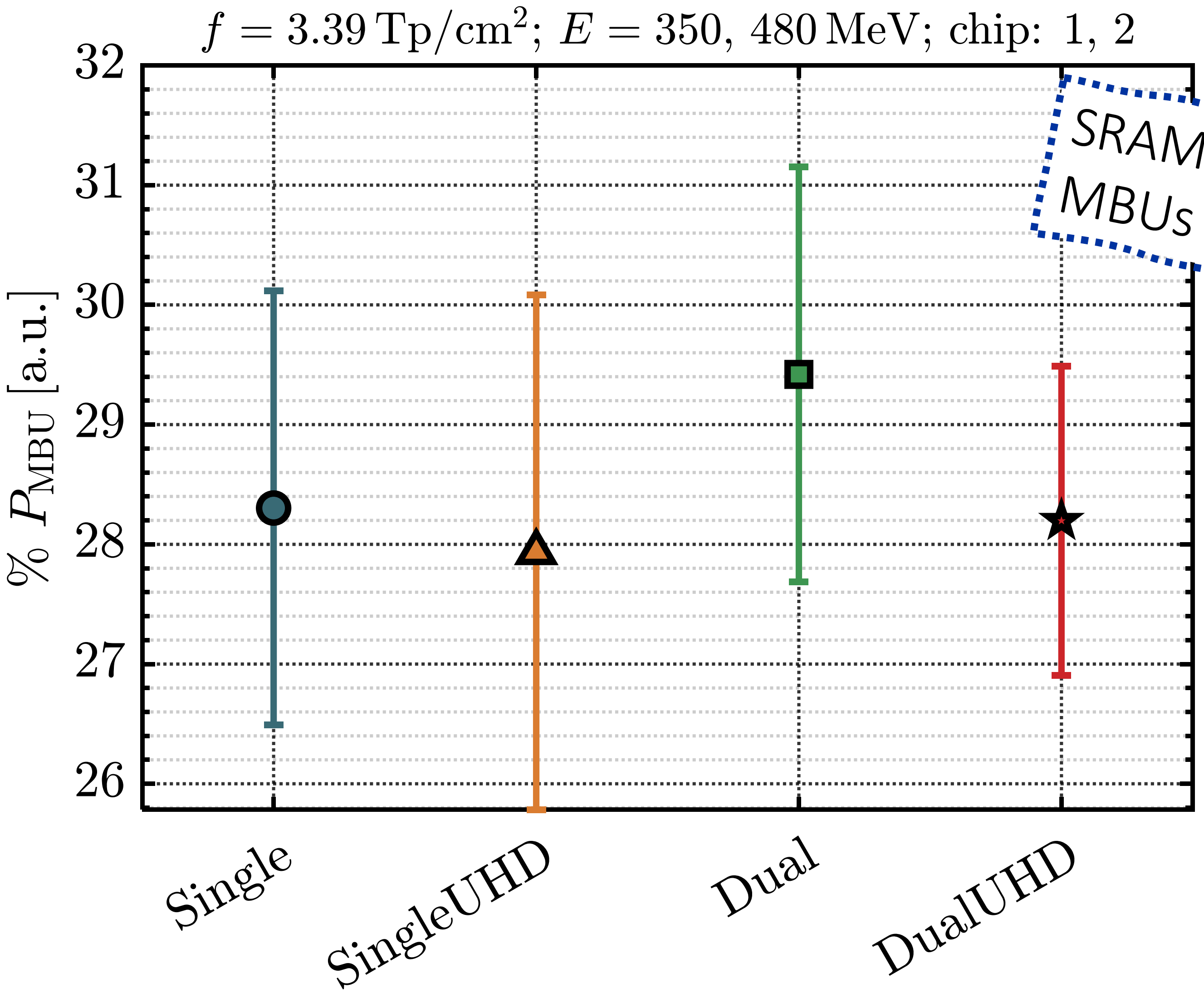


TRIPLICATION

(widely used to prevent SEU)





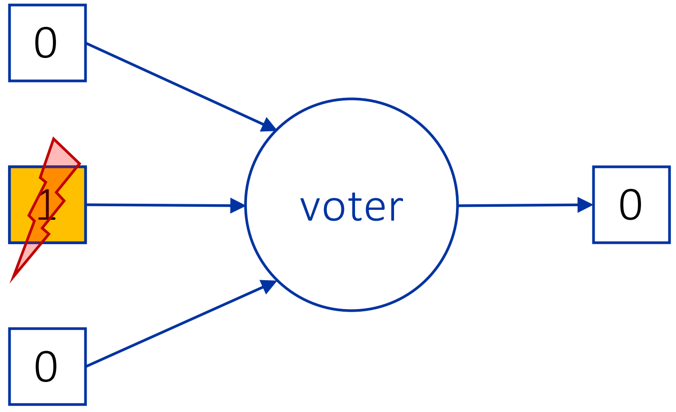


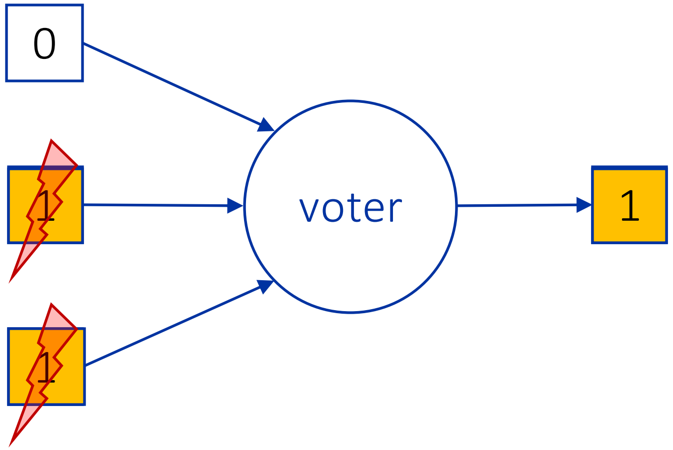
SRAM 28nm irradiated with protons:
MBUs correspond to ~30% of the total errors

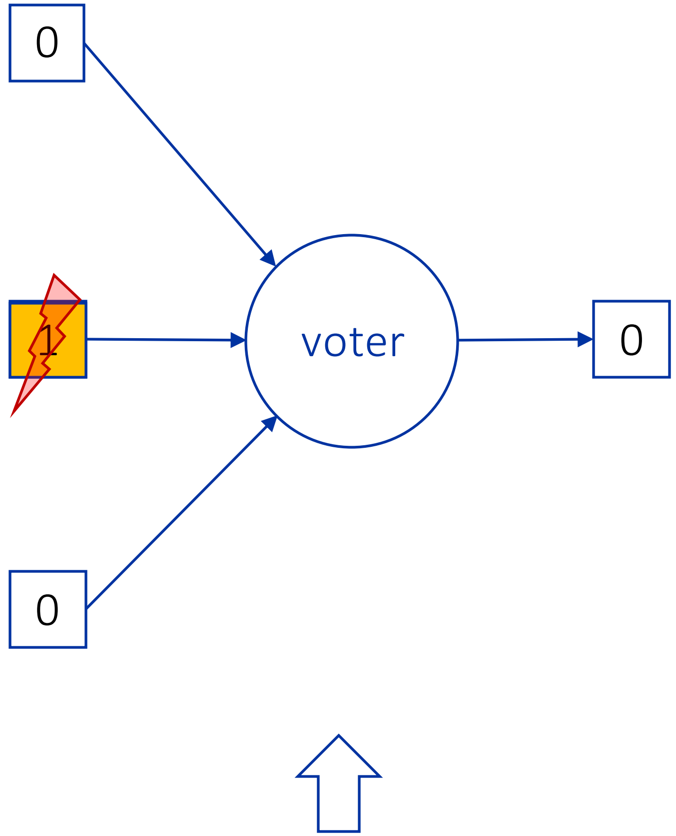
G. Borghello, et al., Single Event Effects characterization of a commercial 28 nm CMOS technology, TWEPP 2023

TRIPLICATION

(widely used to prevent SEU)

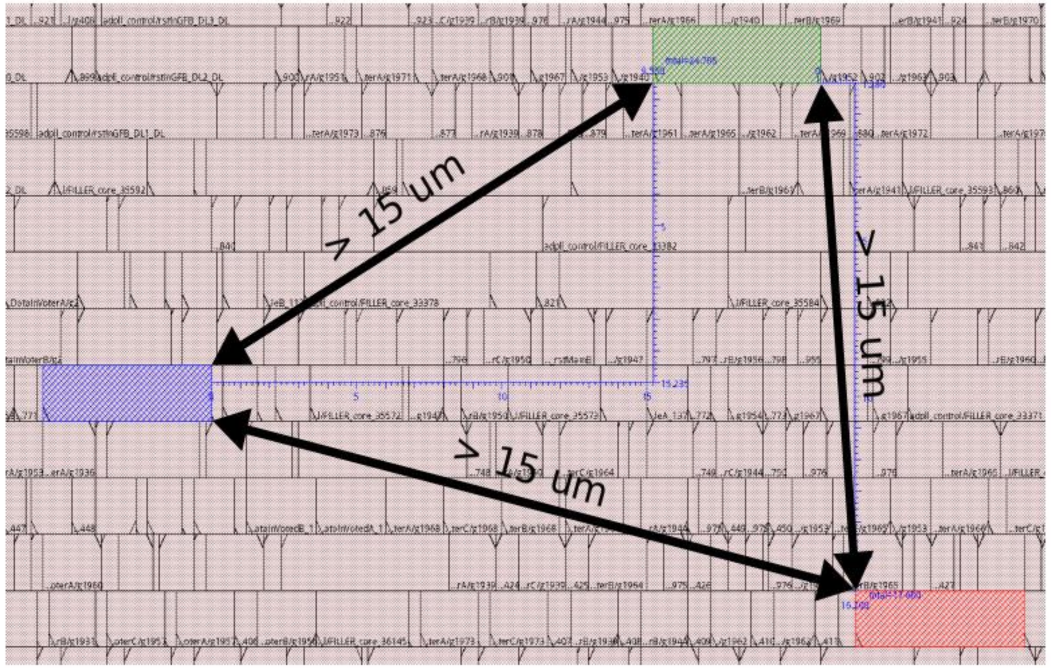






physical distance among triplicated cells reduces the risk of MBU!

15 µm typically used
in 65nm technology

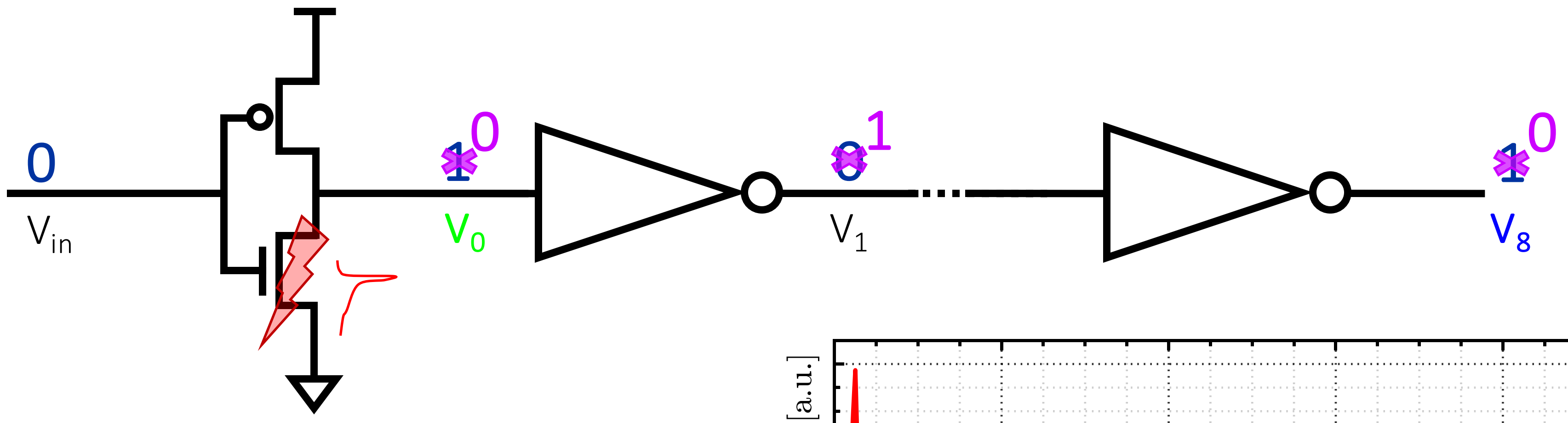


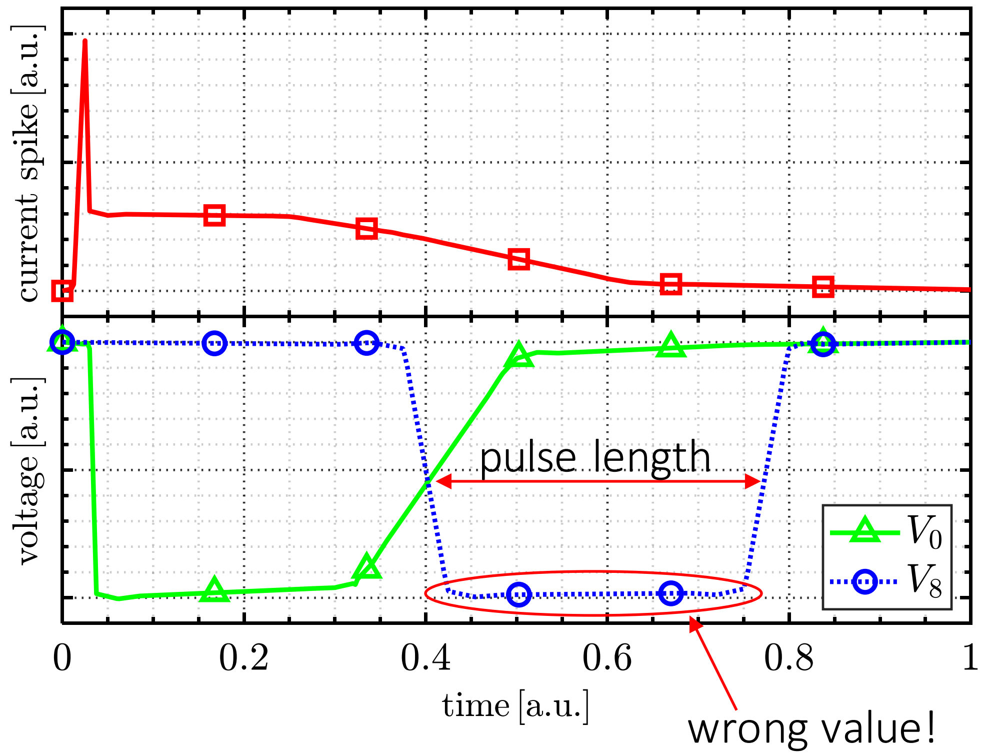
Stefan Biereigel: Investigations on Multi-Bit Upsets in 65nm CMOS (https://indico.cern.ch/event/959655)

most likely 15 µm is an overestimation (see https://indico.cern.ch/event/959655).

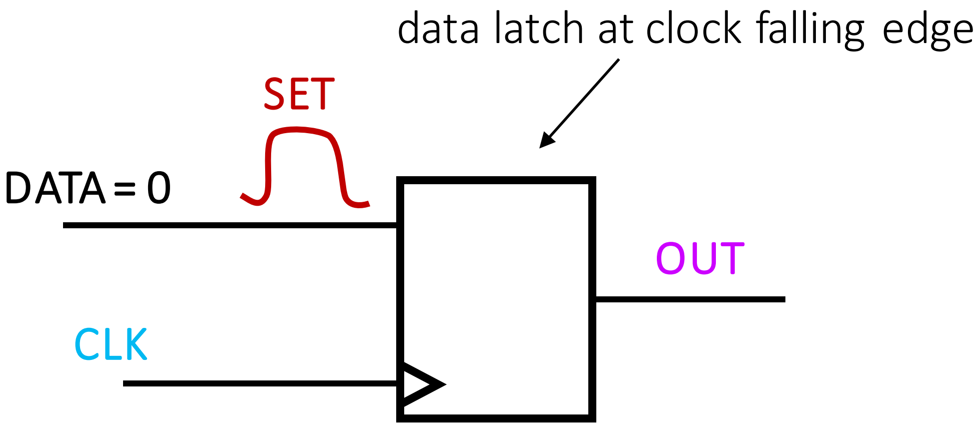
Recent measurements in 28nm showed that ~6um are enough to prevent MBU
(G. Borghello, et al., *Single Event Effects characterization of a commercial 28 nm CMOS technology*, TWEPP 2023).

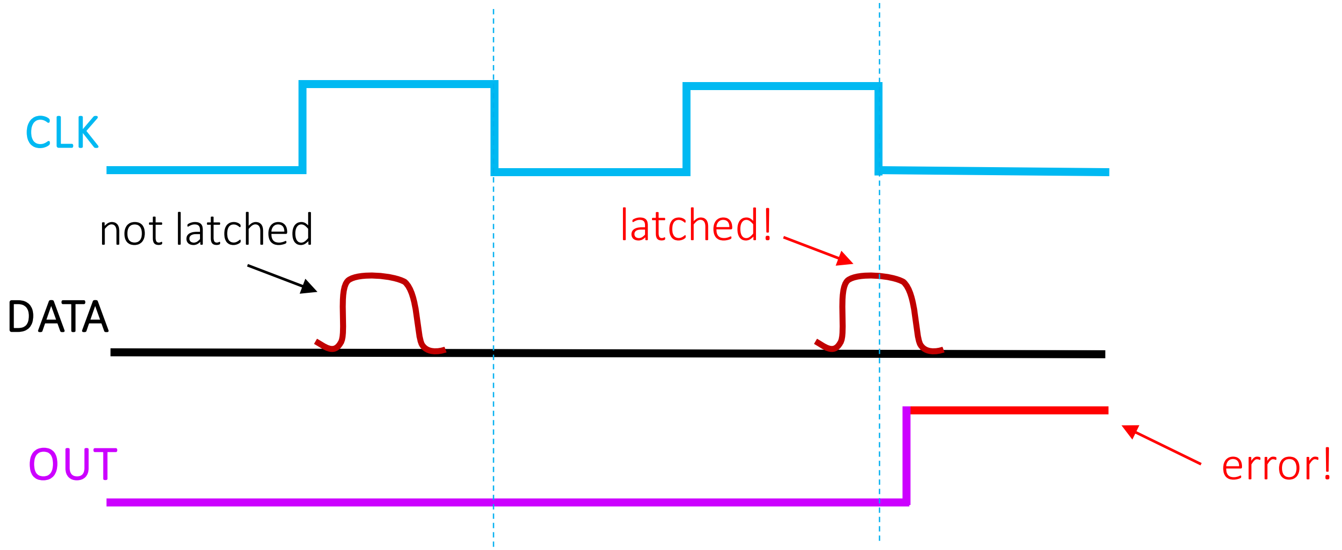
single-event transient



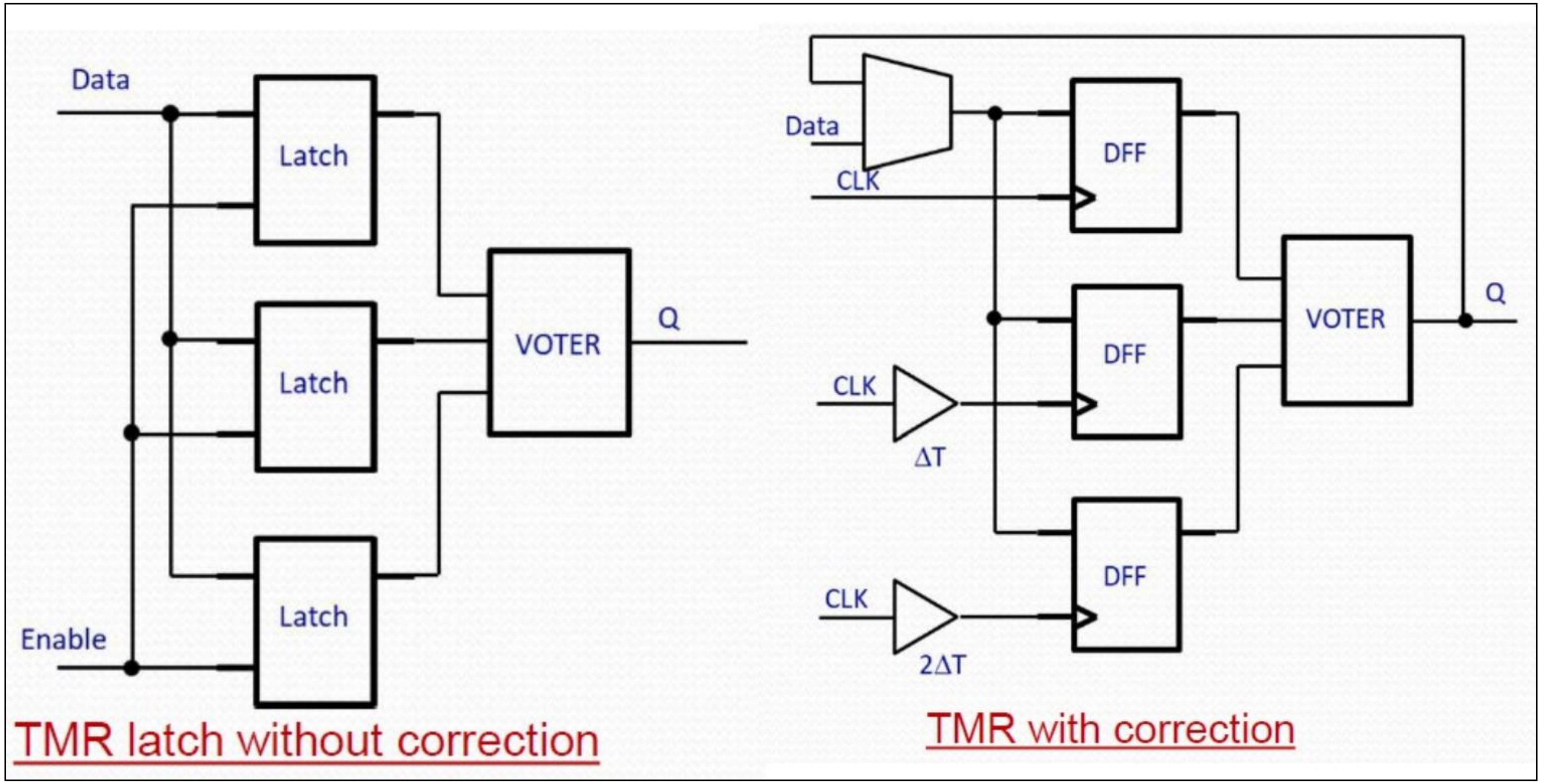


V. Ferlet-Cavrois, L. W. Massengill and P. Gouker, "Single Event Transients in Digital CMOS—A Review," in IEEE Transactions on Nuclear Science, vol. 60, no. 3, pp. 1767-1790, June 2013, doi: 10.1109/TNS.2013.2255624.


data latch at clock falling edge
SET
DATA = 0
OUT
CLK

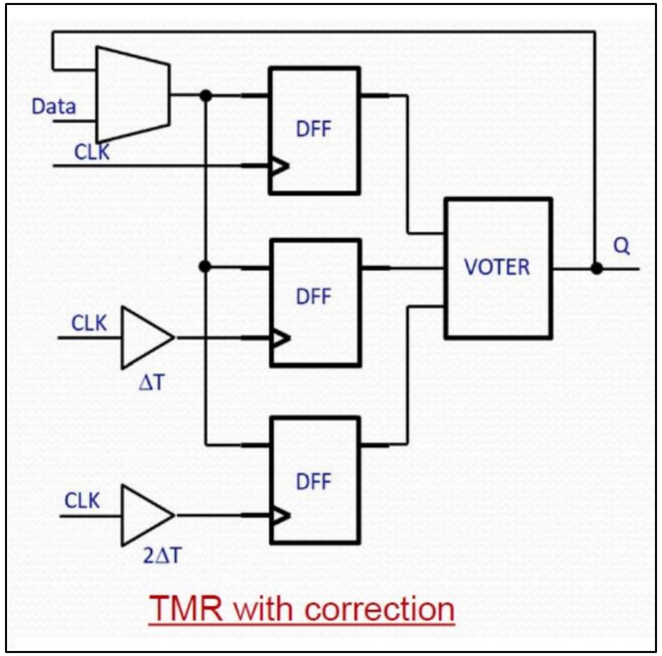

CLK
not latched
latched!
DATA
OUT
error!

RD53*: triplicated clock tree with skew for SET filtering

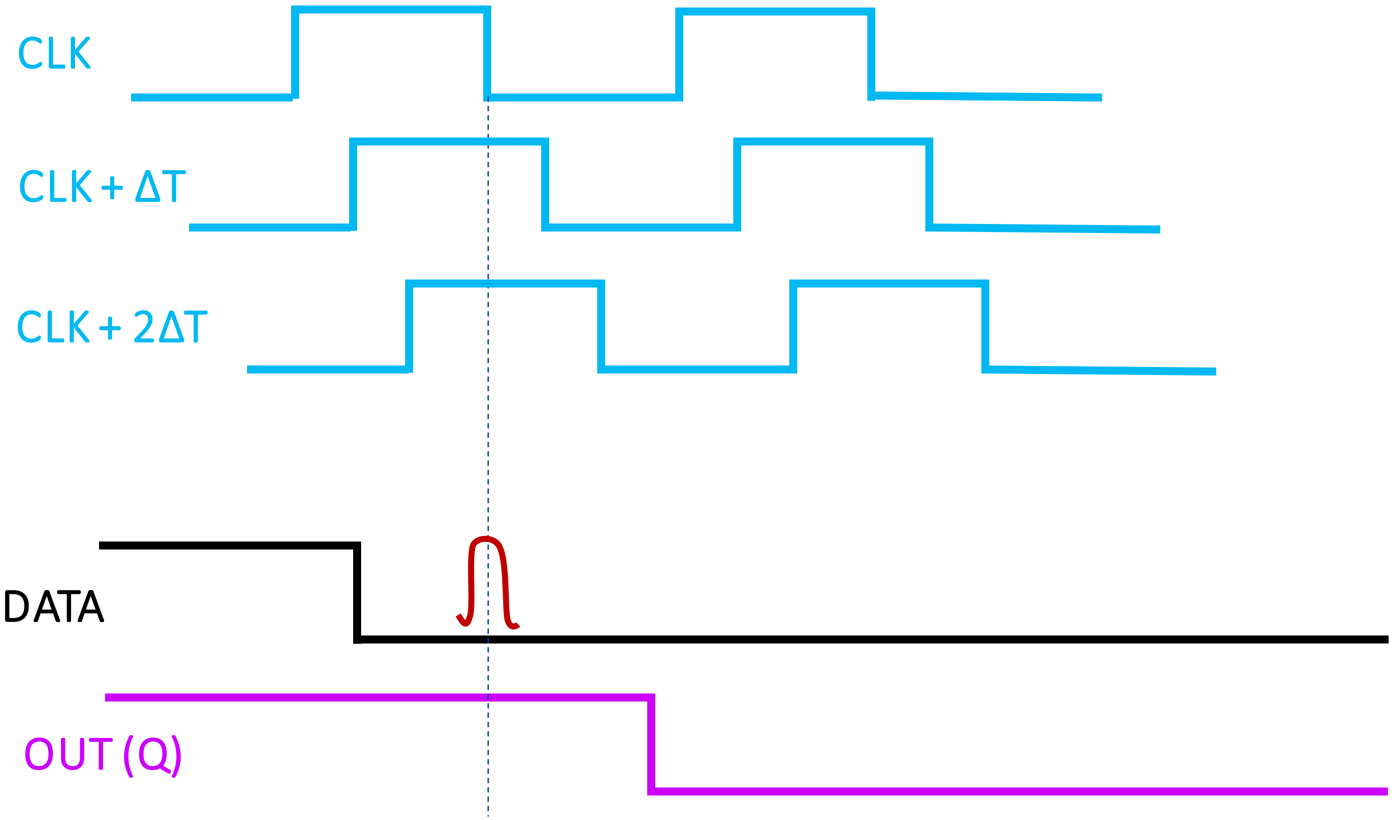


https://indico.cern.ch/event/1038992/contributions/4363708/attachments/2256379/3829070/LHCC_RD53_June2021.pdf

*readout chips for the ATLAS and CMS pixel detector (https://rd53.web.cern.ch/)



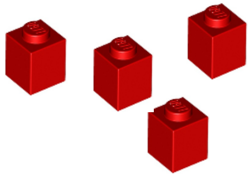
TMR with correction



This hardening techniques requires the knowledge of the SET pulse length!

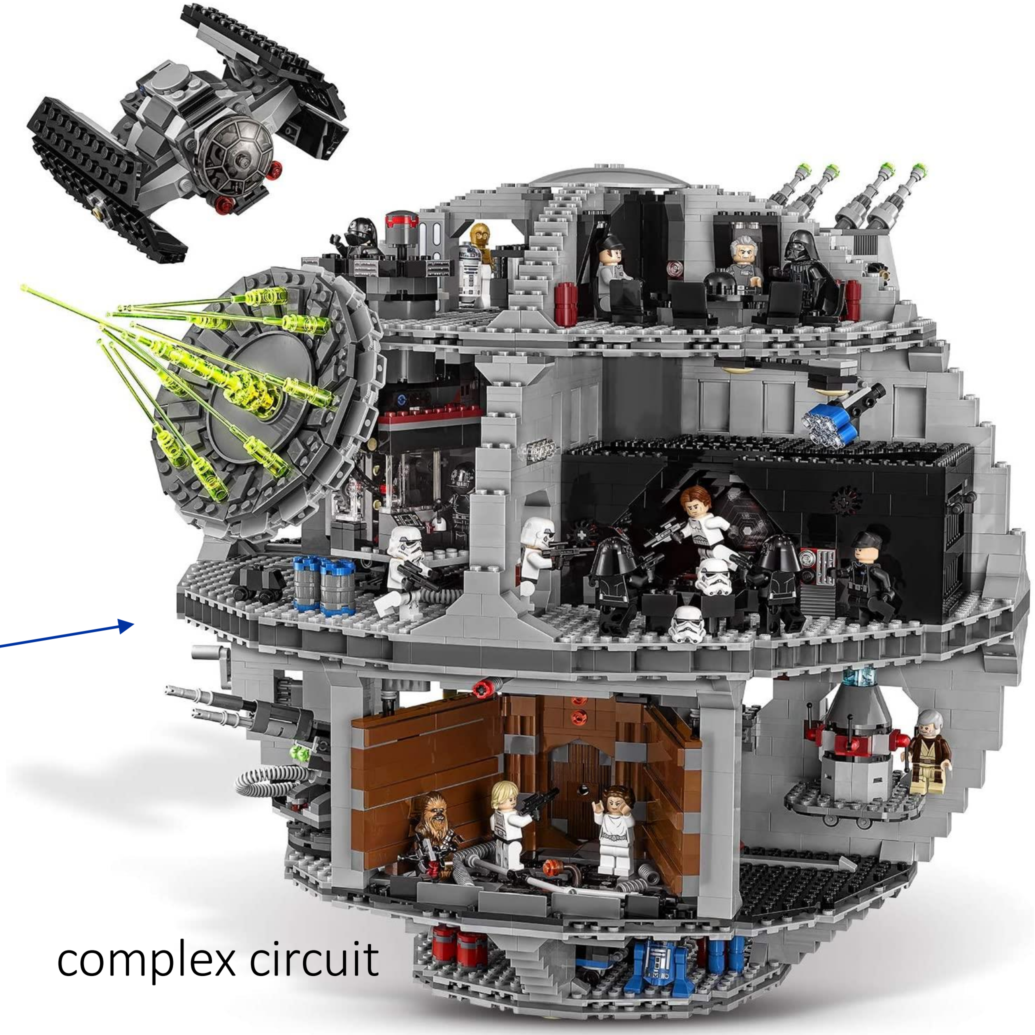
typical pulse length ~100ps

MOS (Metal-Oxide-Semiconductor) transistors are the building blocks of any complex integrated circuit!



MOS transistors

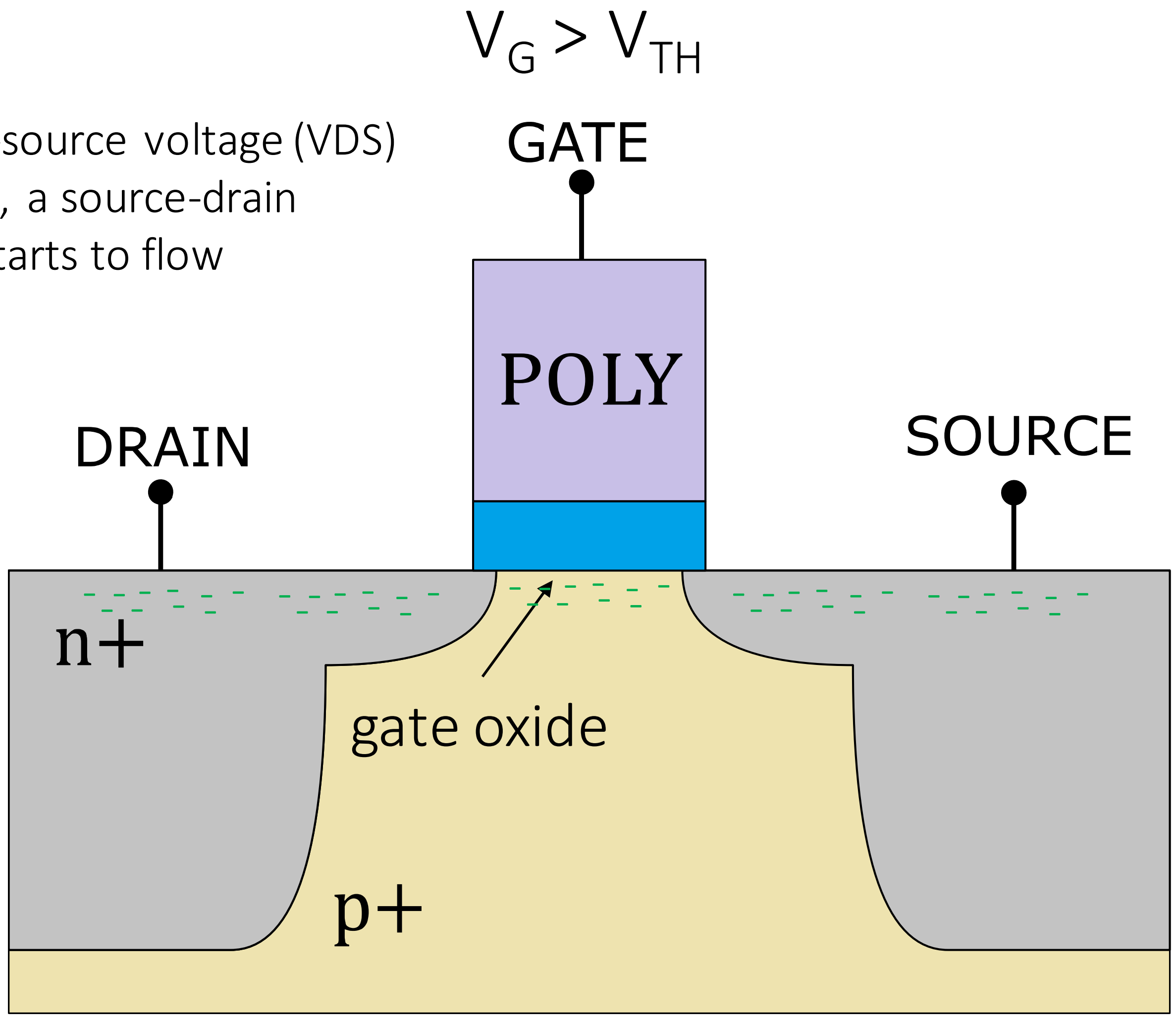
a lot of work

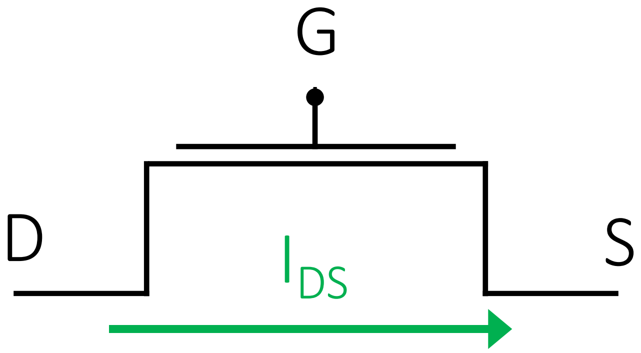


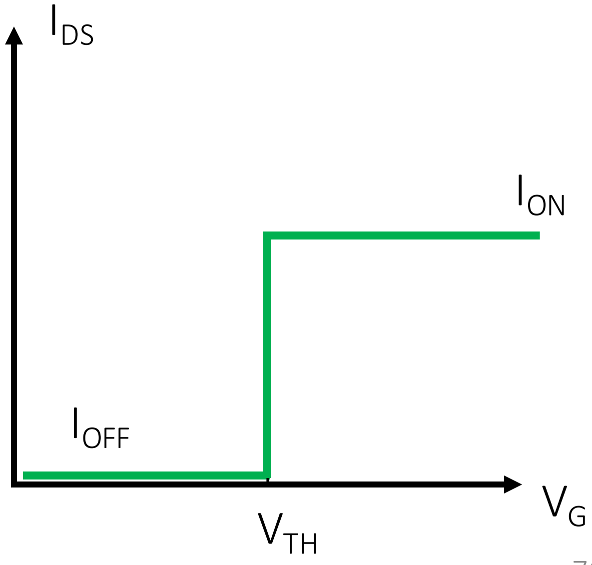
complex circuit

MOS transistors behaves (ideally) like switches controlled by voltage applied to the gate terminal

If a drain-source voltage (VDS) is applied, a source-drain current starts to flow





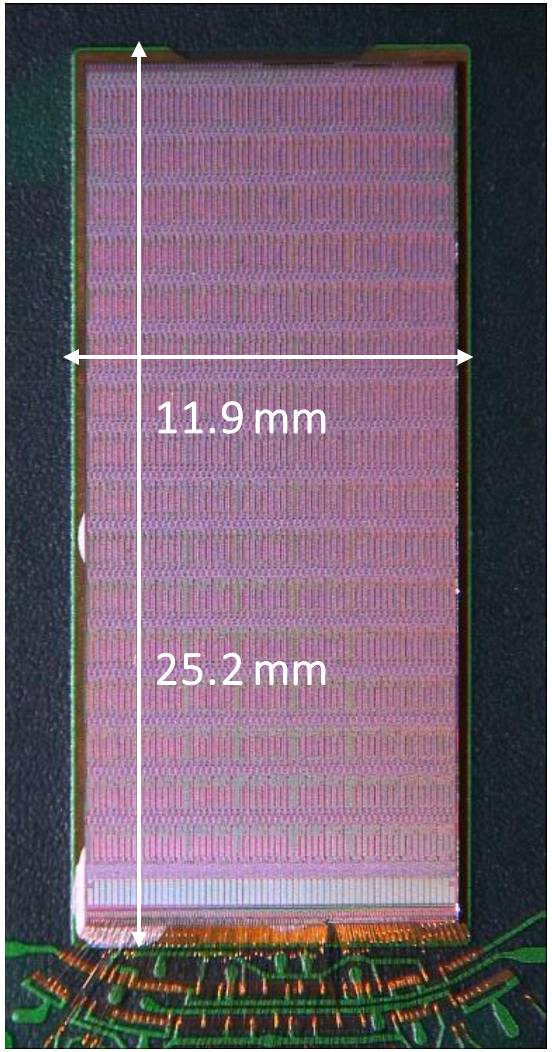


example:

MPA (Macro Pixel ASIC)

For **CMS** outer tracker:

~1.5M of MOS transistors

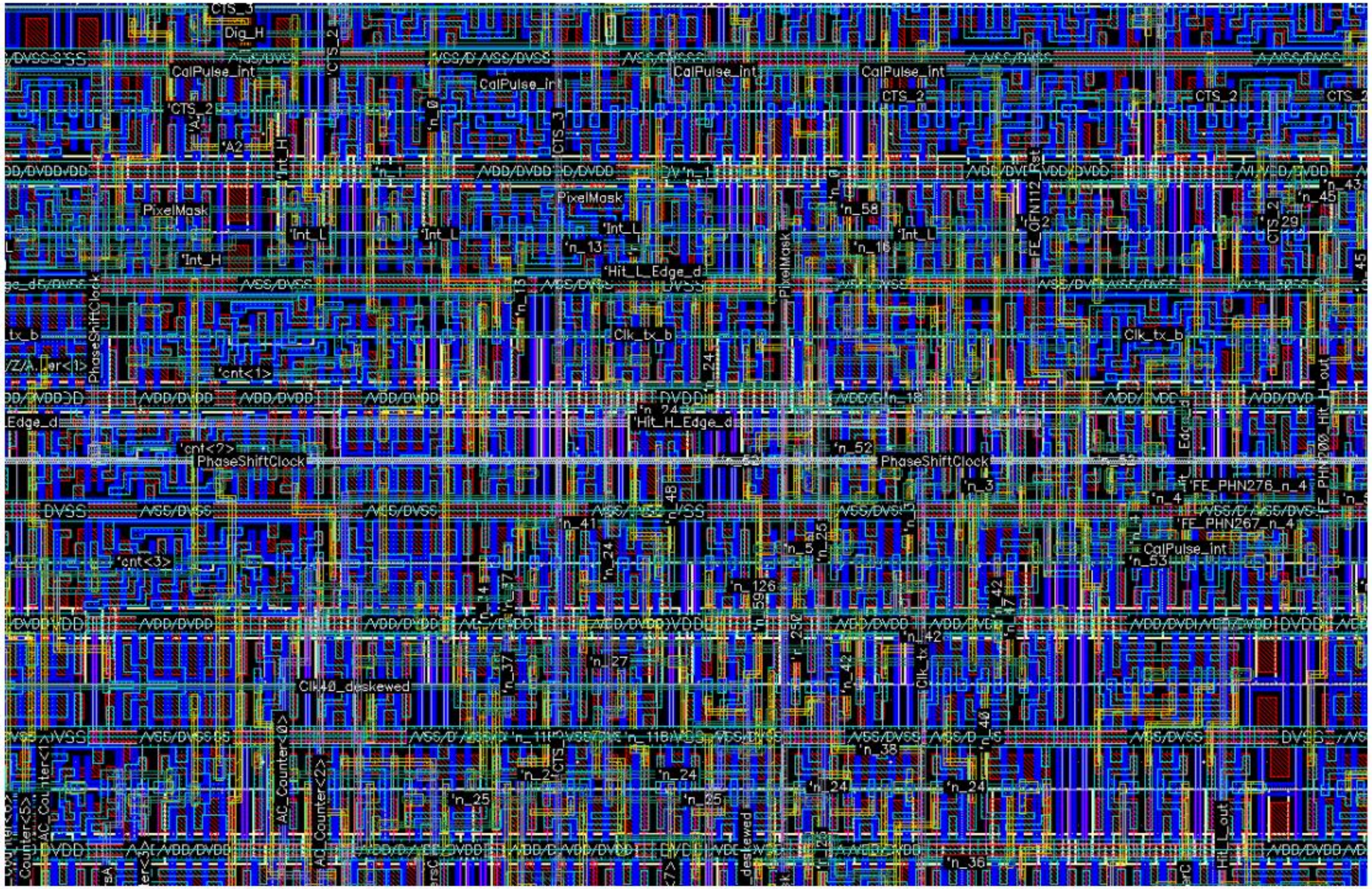


Courtesy of Davide Ceresa, CERN (EP-ESE-ME section)

Billions of transistors for each experiment!

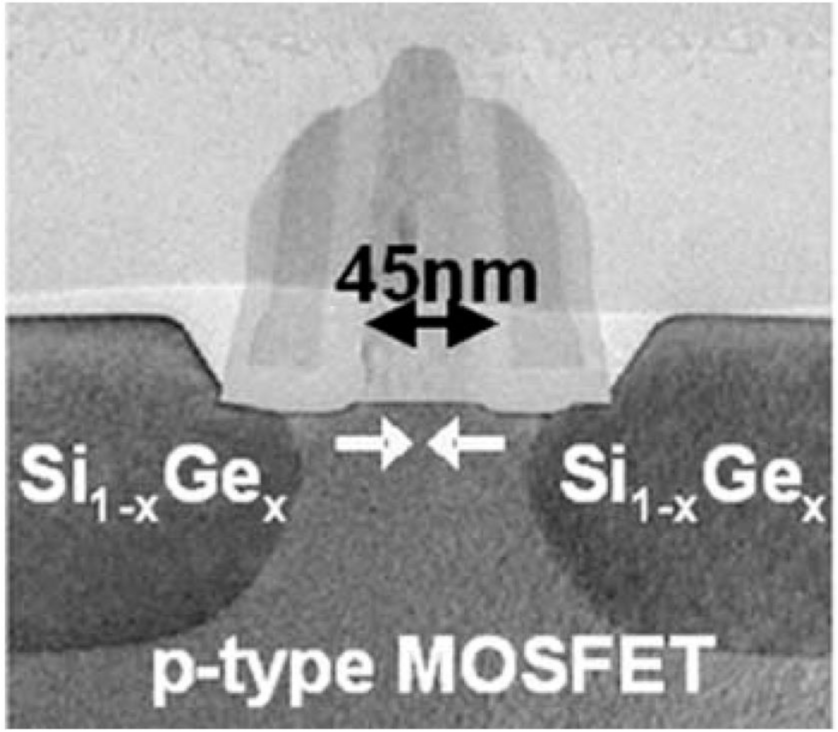
https://espace.cern.ch/CMS-MPA/SitePages/Home.aspx

Schematic view of thousands of transistors interconnected by metal lines



to fit millions of transistors in a chip, MOS must be small!

example of a real MOS device



S. E. Thompson *et al*., "A logic nanotechnology featuring strained-silicon," in *IEEE Electron Device Letters*, vol. 25, no. 4, pp. 191-193, April 2004

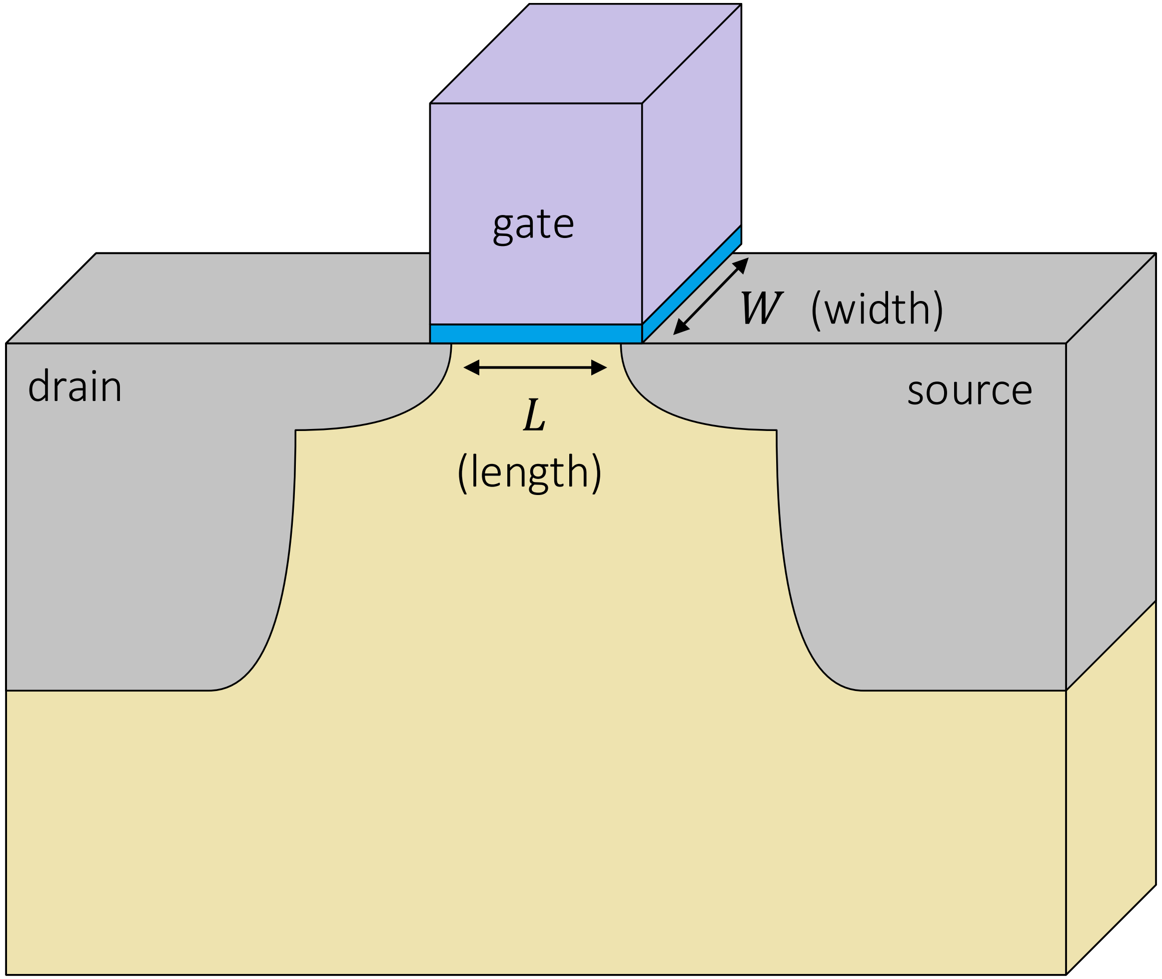
technology scaling

to reduce the minimum size of MOS transistors, several innovation/changes are introduced in the fabrication process

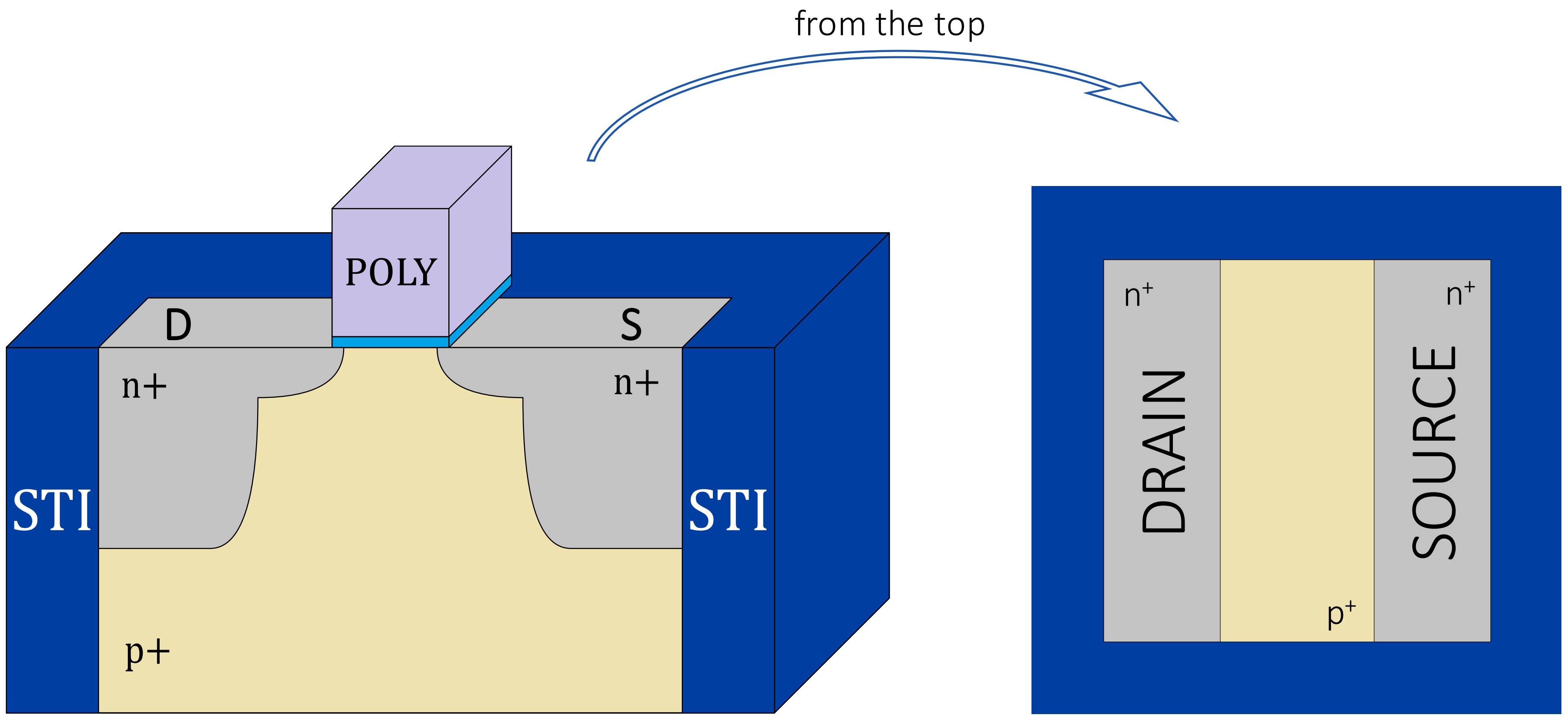
CMOS technology node

identified with the minimum feature size available*
(e.g., 28nm technology node -> minimum feature size ~28nm)

*The name of recent technology nodes (e.g., 22 nm, 16 nm, etc..) refer purely to a specific generation of chips made in a particular technology. It does not correspond to any feature size. Nevertheless, the name convention has stuck (https://en.wikichip.org/wiki/technology_node).



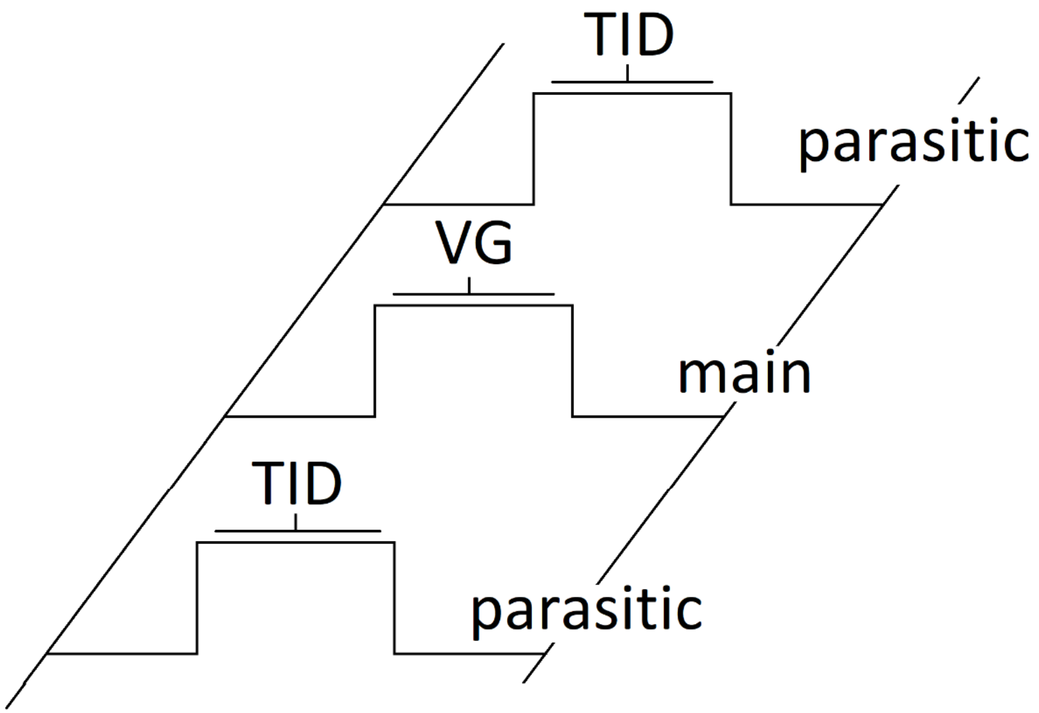
$$I_D \propto \frac{W}{L}$$

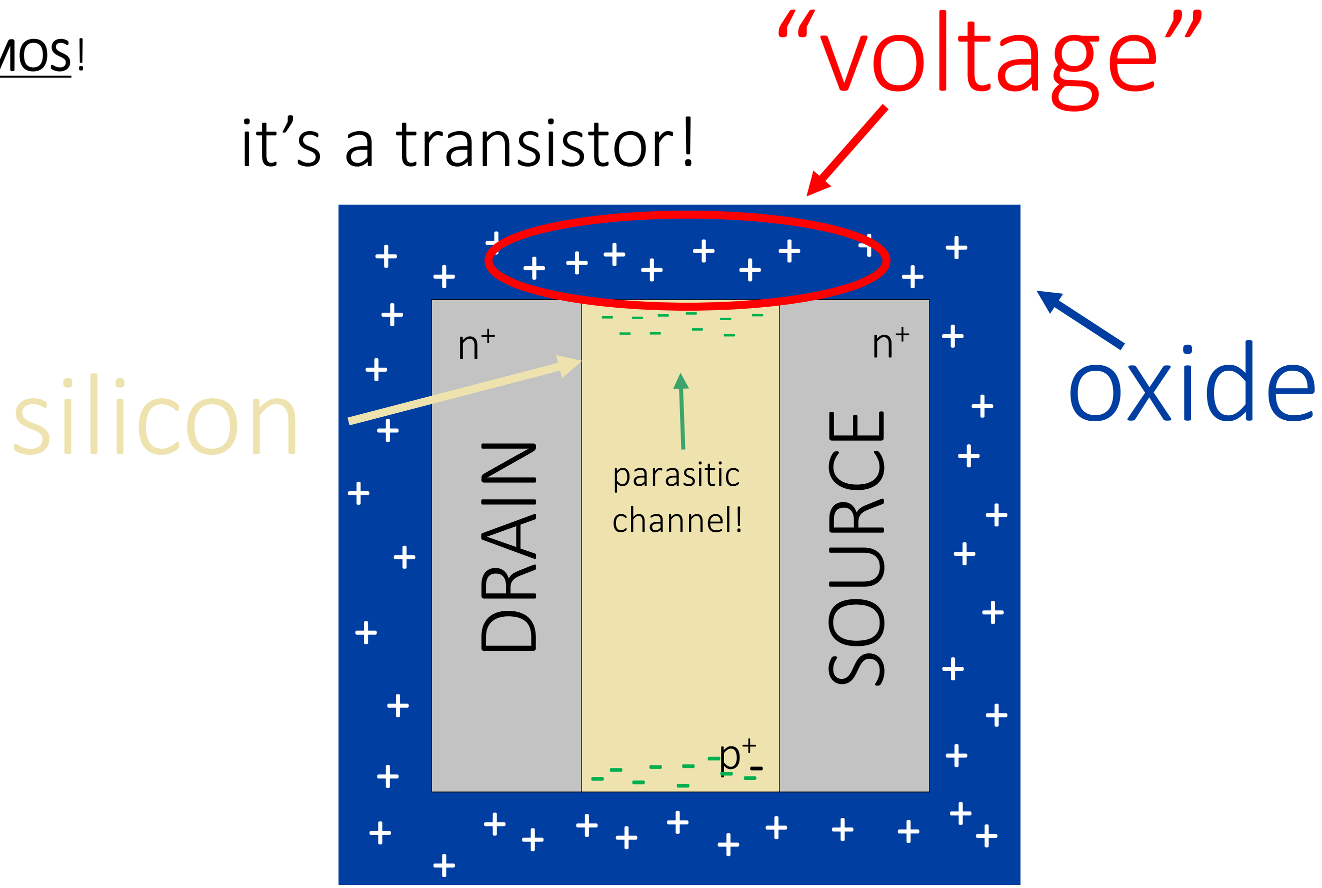

from the top
POLY
D
S
n+
n+
STI
STI
p+
n^+
n^+
DRAIN
SOURCE
p^+

TID-induced positive charge in the oxide

we are only interested in the charge that faces the channel

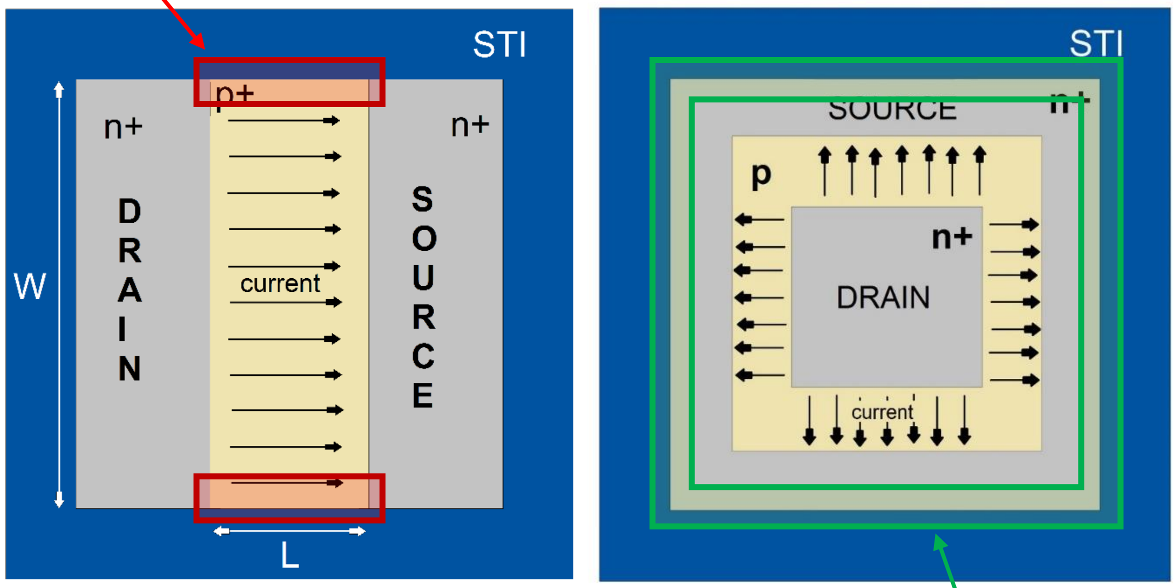
positive charge attracts electrons -><u>problem only in nMOS</u>!





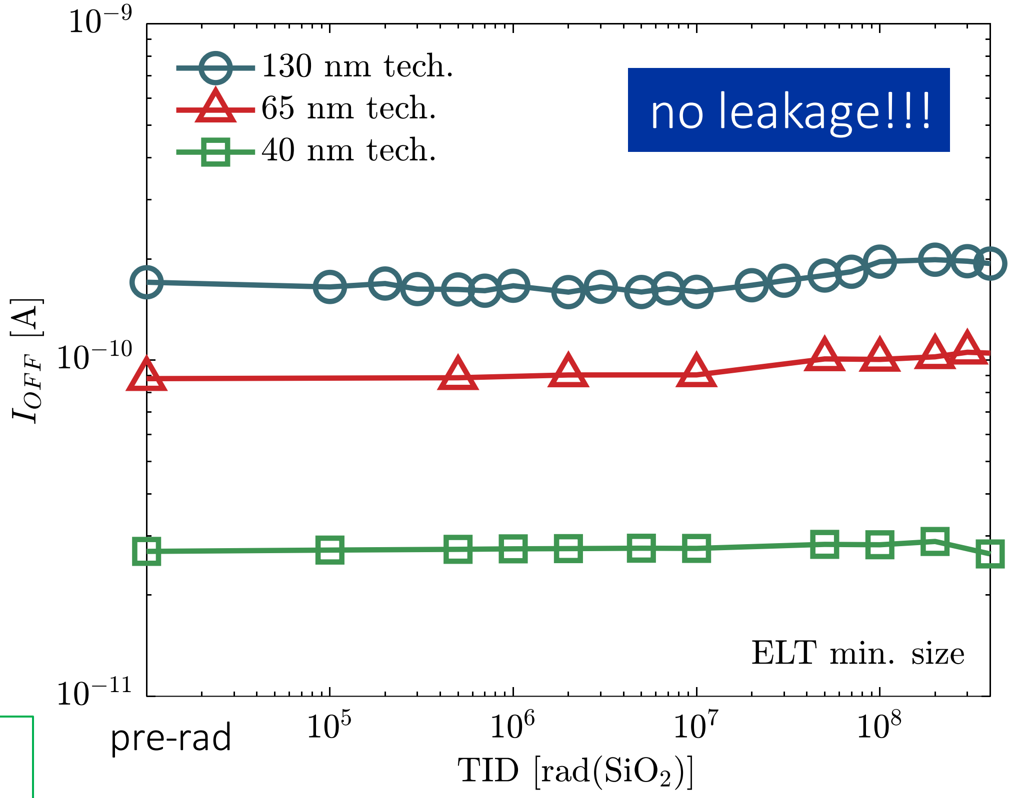
NOT AVAILABLE IN 28nm and smaller nodes!

the STI faces the channel



MOSFET TOP VIEW

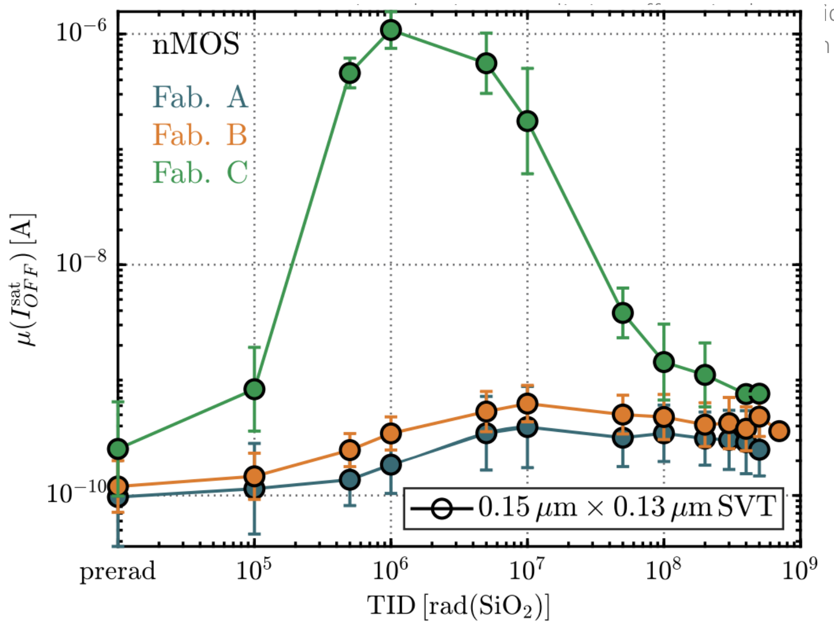
the STI does not face the channel!

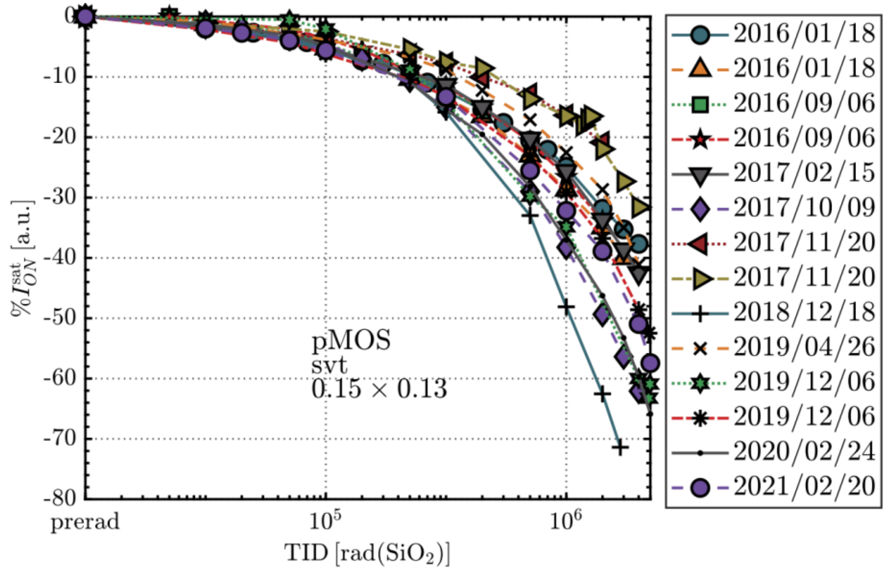


radiation-induced variability

TID effects are affected by:

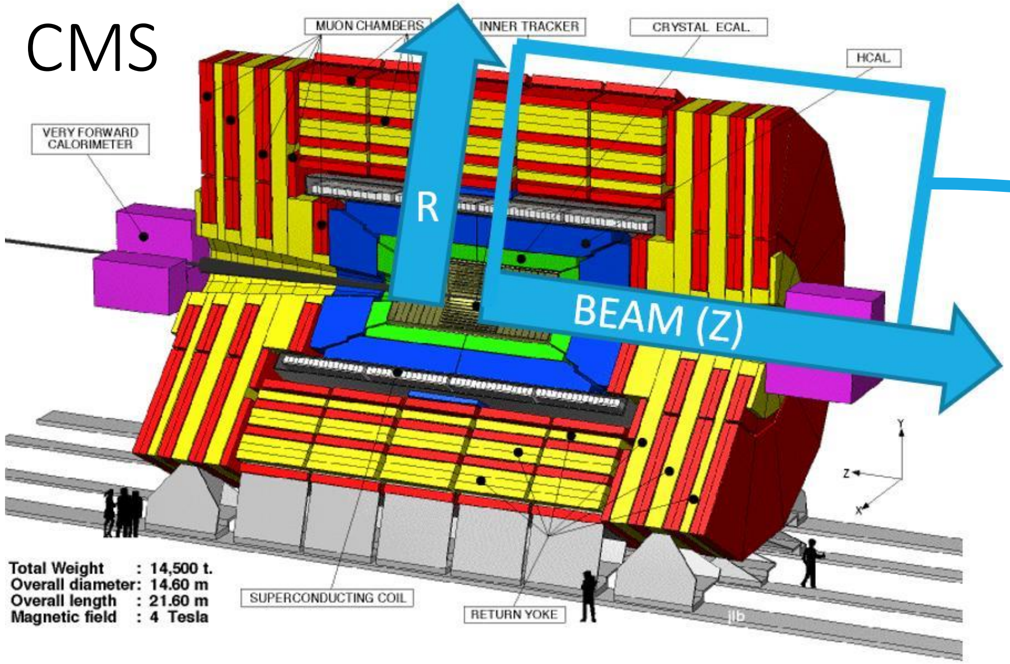
- technology-to-technology variability
- manufacturer-to-manufacturer variability
- fab-to-fab variability
- chip-to-chip variability
- lot-to-lot variability
- transistor-to-transistor variability



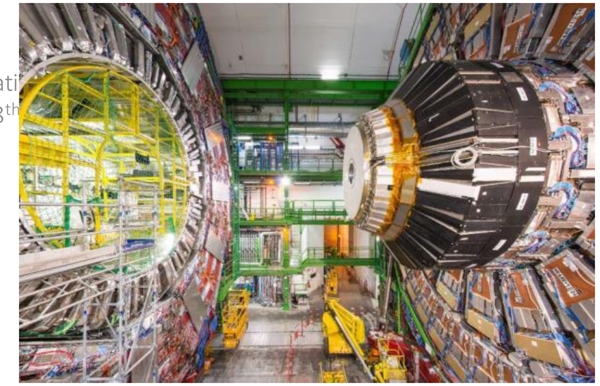


Termo, G., Borghello, G., Faccio, F., Michelis, S., Koukab, A., & Sallese, J. M. (2023). "Fab-to-fab and run-to-run variability in 130 nm and 65 nm CMOS technologies exposed to ultra-high TID". *Journal of Instrumentation*, 18(01), C01061.

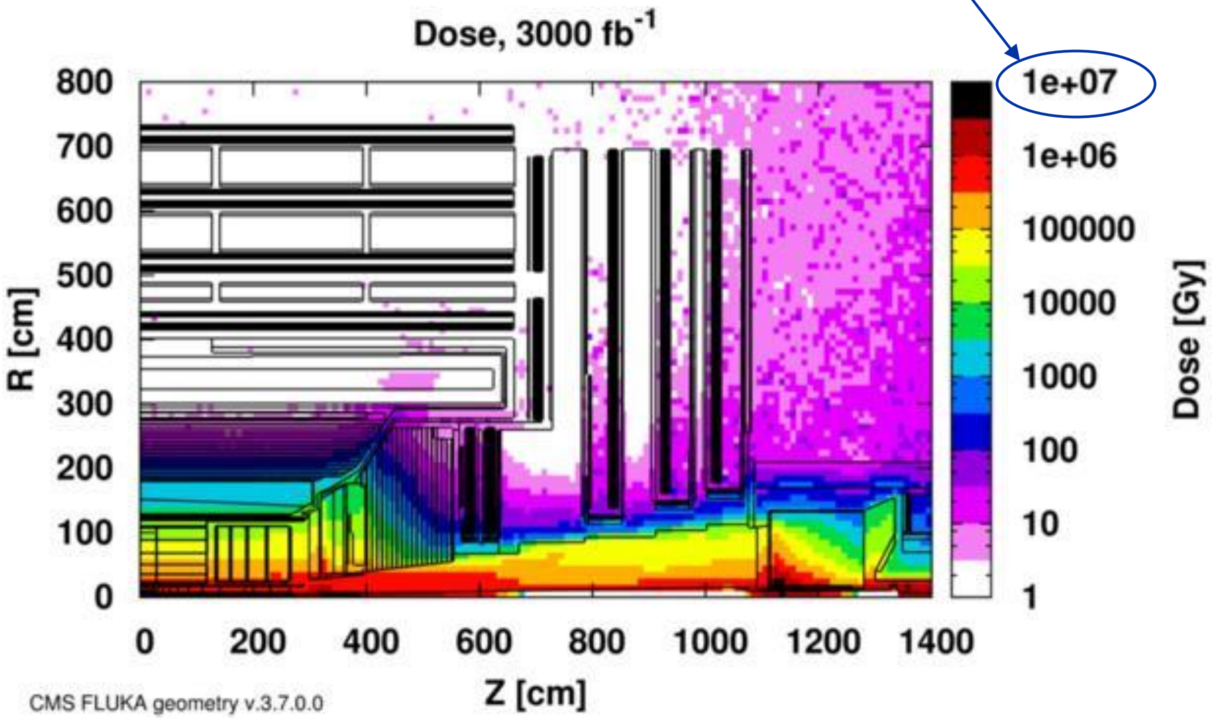
CMS



B. Schmidt. “The High-Luminosity upgrade of the LHC: Physics and Technology Challenges for the Accelerator and the Experiments.” In: Journal of Physics: Conference Series 706.2 (2016), p. 022002. url: http://stacks.iop.org/1742-6596/706/i=2/a=022002

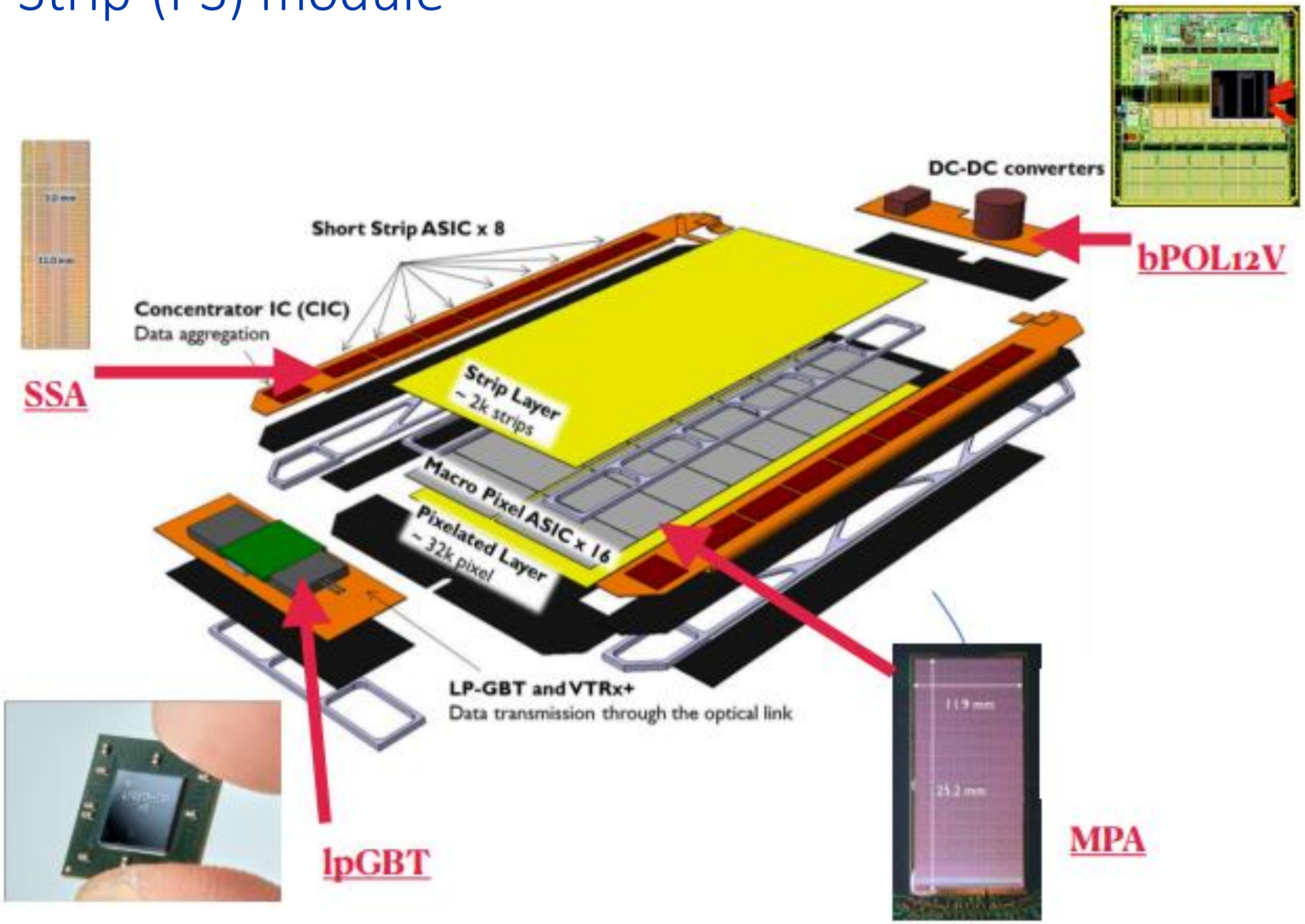


10 MGy = 1 Grad!



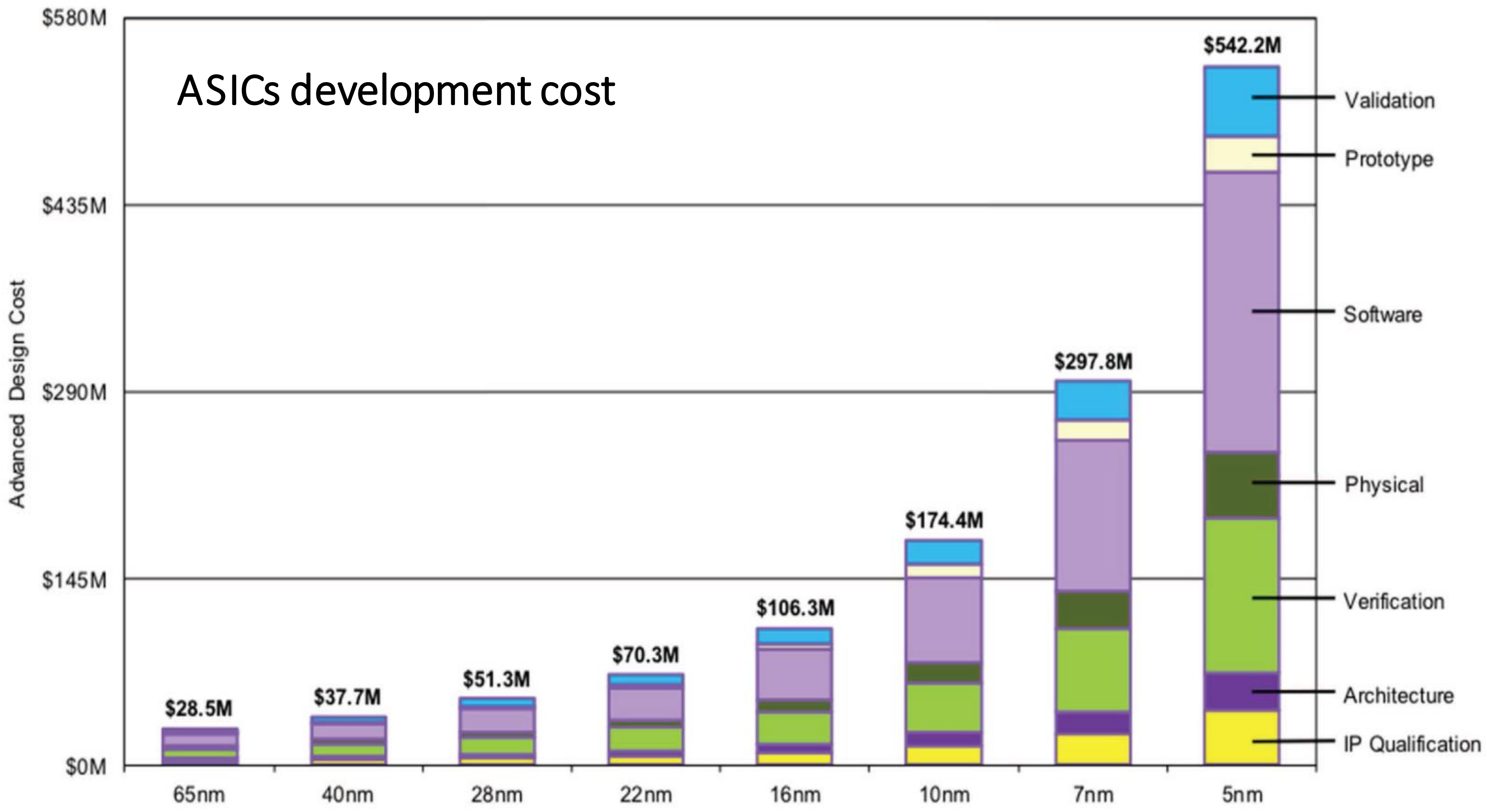
Sophisticated electronics near the interaction point -> very high radiation levels!!

CMS Pixel-Strip (PS) module



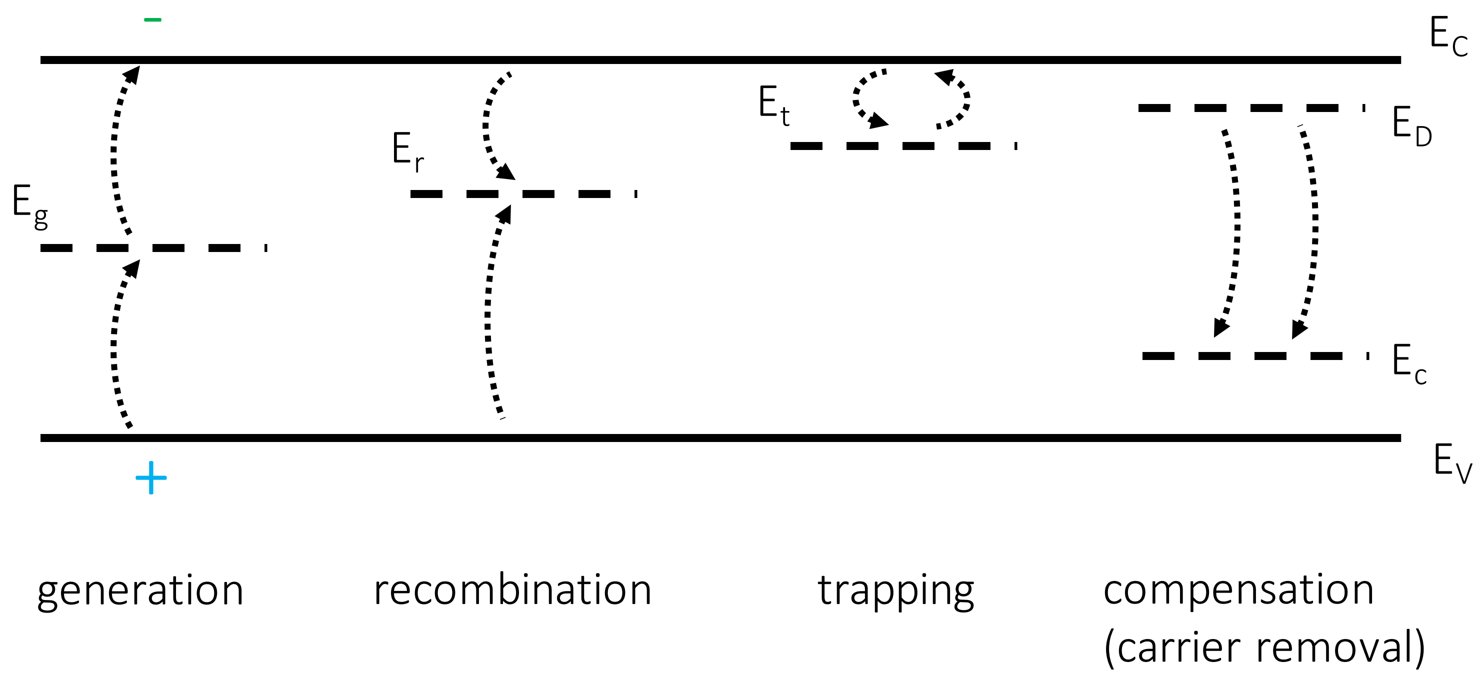
why aren't we testing smaller technologies?

many reasons but mainly…



Chip Design and Manufacturing Cost under Different Process Nodes. According to the survey from the *International Business Strategy Corporation (IBS),* the increase of design cost for each generation technology has exceeded 50% after 22 nm process, including EDA, design verification, IP core, tape-out, and so forth.
https://www.extremetech.com/computing/272096-3nm-process-node

physical mechanisms of DD-induced degradation



[1] J. R. Srour, C. J. Marshall and P. W. Marshall, "Review of displacement damage effects in silicon devices," in *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 653-670, June 2003, doi: 10.1109/TNS.2003.813197.
[2] Oldham, Timothy R. "Basic mechanisms of TID and DDD response in MOS and bipolar microelectronics." *NSREC Short Course* (2011).
[3] J. R. Srour and J. W. Palko, "Displacement Damage Effects in Irradiated Semiconductor Devices," in *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1740-1766, June 2013, doi: 10.1109/TNS.2013.2261316.

Non-ionizing energy loss (NIEL) and damage factor

NIEL [MeV/(mg/cm^2)] is the amount of energy “used” to displace atoms

NIEL scaling (hypothesis):

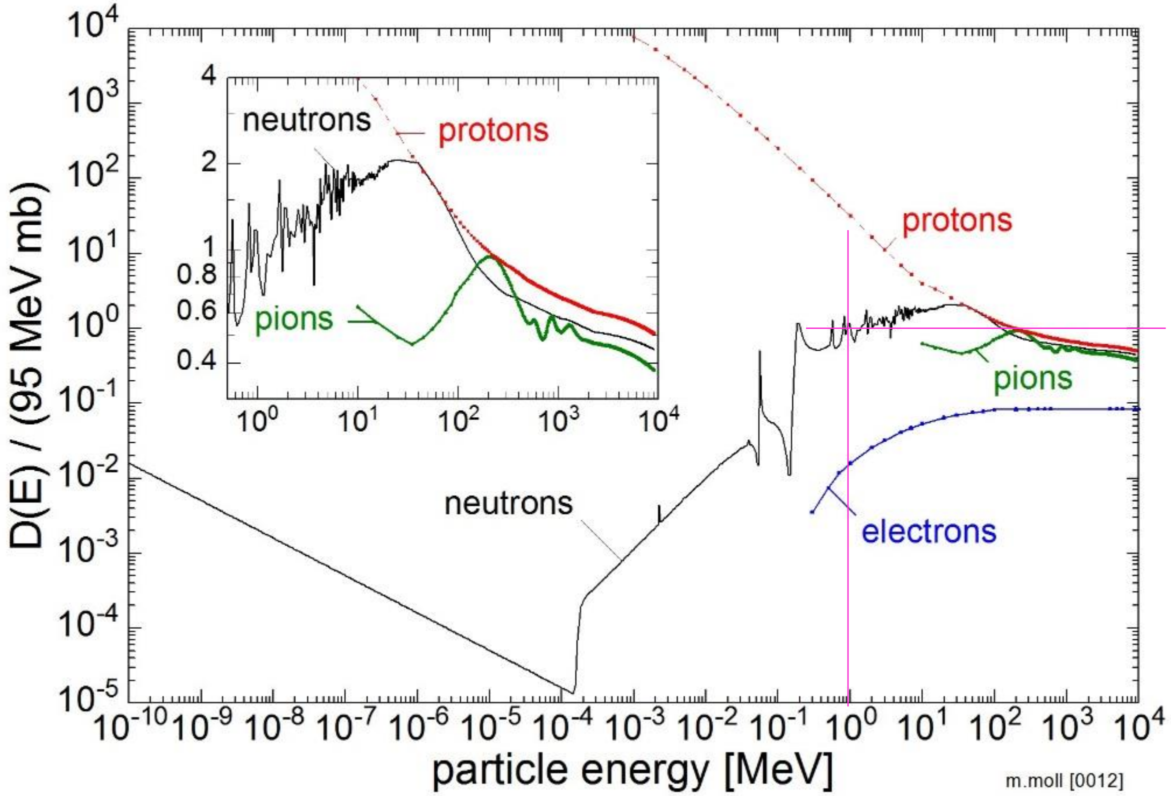
damage effects on devices only depend on NIEL and not on the type/energy of the particle
i.e., different particles with the same NIEL should produce the same macroscopic effect

$$D(E) = NIEL \times A/N_A$$

A: molar mass, N_A Avogadro’s number

Normalization of radiation fields to
1 MeV neutron equivalent damage (n_{eq})

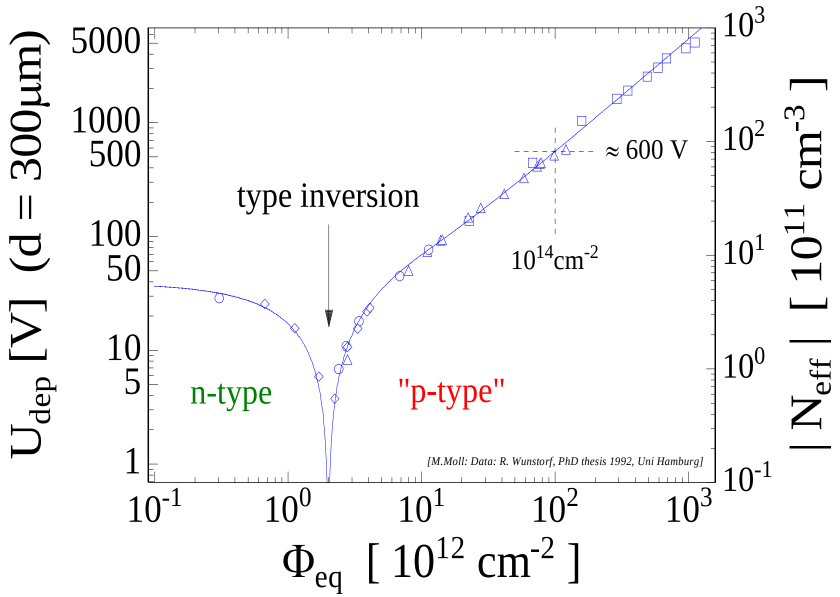
$$\Phi_{eq} = \kappa_x \, \Phi_x$$



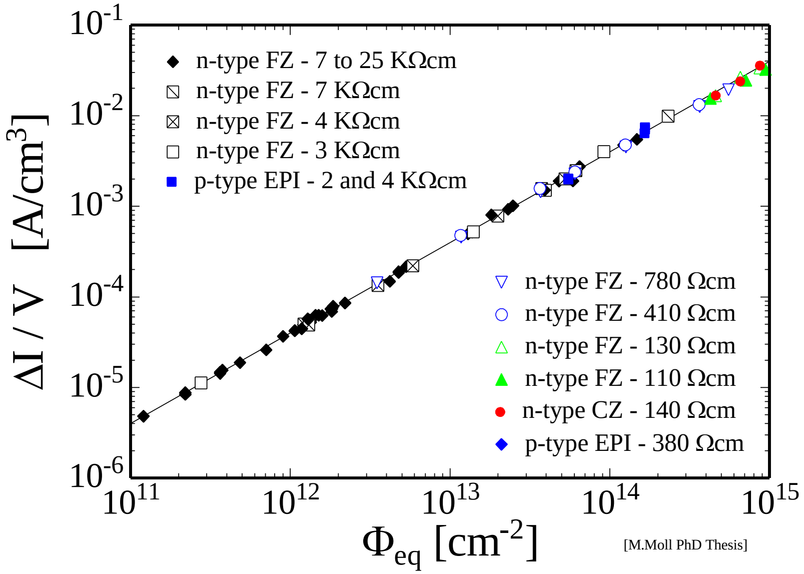
Displacement Damage in Silicon https://rd50.web.cern.ch/NIEL/

Moll, Michael. "Displacement damage in silicon detectors for high energy physics." *IEEE Transactions on Nuclear Science* 65.8 (2018): 1561-1582
A. Vasilescu and G. Lindstroem, Displacement damage in Silicon, on-line compilation: http://sesam.desy.de~/gunnar/Si-dfuncs

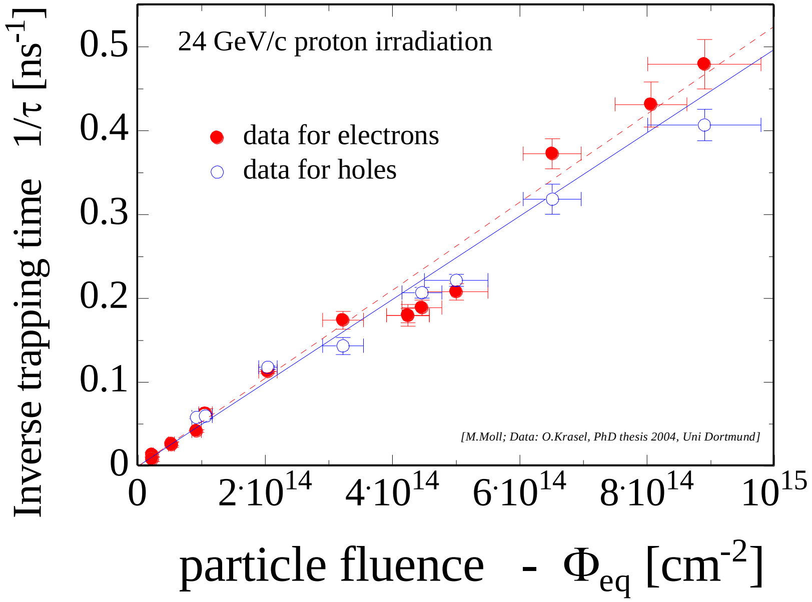
- Macroscopic bulk effects



Depletion Voltage (N_{eff})



Leakage Current



Charge Trapping

Moll, Michael. "Displacement damage in silicon detectors for high energy physics." IEEE Transactions on Nuclear Science 65.8 (2018): 1561-1582.